

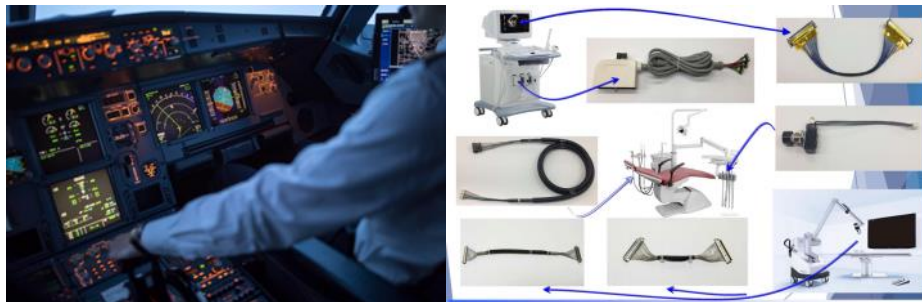


[www.usmarunitech.com](http://www.usmarunitech.com)

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(<https://www.marunix.co.jp/>)



Display :  
Embedded  
Cable  
Assemblies



### **VESA® : eDP or LVDS**

- High speed differential signal transfer cables
- Shielded—Fine Pitch capabilities (IATF)
- Micro-coax or Twisted Pair technology
- Japanese QA Management
- Production in China



**MARUNIX Co. Ltd**    Established: September 1, 1973    6794-2 Masubayashi Koshigaya-city, Saitama, Japan  
Business: Cable Assembly Fabricator including custom mechanical components, this plant now produces gaming cables.  
**MARUNIX presently employs ~6,000 people worldwide**

**Dongguan Marunix Electronics Co., LTD.**  
Established: September 1994    Hujie Town, Dongguan City, Guangdong China    ISO9001/2000\_ISO14000, UL, CSA  
Business: Discrete Wire cable assemblies, Twisted Pair Technology for general signal transfer like LVDS & Automotive  
Present employment ~500 people

**Marunix Electronics (Nanjing) Limited**  
Established: June 2002    Nanjing, Jiangsu, China  
ISO9001/2000\_ISO14000, UL, CSA  
Business: Discrete Wire cable assemblies, Twisted Pair Technology for general signal transfer like LVDS & Automotive  
Also produces Micro-coax cable assemblies.    Present employment ~600 people

**Shaoguan Marunix Electronics Limited**  
Established: October 2000    Shaoguan City, Guangdong, China  
ISO9001/2008\_ISO14000/2004, UL, IATF16949/2016  
Business: High speed, Fine Pitch (0.25mm –SGC48) Micro-Coax RoHS cable assemblies & for Medical Ultrasound Transducer  
Customers: **Sony, Cannon, NEC, Fujitsu, Epson, Ricoh, DJI, LG, BYD,** & more. Present employment ~1000+ people  
**Sony Certified & Cannon Certified Mass production supplier**  
On ~5 Acers with 3 permanent Japanese Managers

**Marunix Hong Kong Limited** - Shatin, NT, Hong Kong

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VESA 16:9 Wide Notebook Panel Standard

Version 3

9 November 2010



**Purpose**

This standard defines the requirements for the standardization of mechanical dimensions and selected electrical interface requirements for 10.1-, 11.6-, 13.3-, 13.4-, 14.0-, 15.6-, 17.3- and 18.4-inch W (wide format) 16:9 panels. The intent of this standard is to help LCD manufacturers and panel consumers to better control panel supply and demand cycles, as panels built to these specifications will be able to be used interchangeably without requiring alterations in product tooling or the display module.

**Summary**

This standard describes the selected electrical interfaces, mechanical dimensions and data formatting for 10.1-, 11.6-, 13.3-, 13.4-, 14.0-, 15.6-, 17.3-, and 18.4-inch wide format (W) 16:9 panels.

**Pin1 Confusion – Mechanical Specifications Defined from Front View of Display Panel**

VESA 16:9 Notebook Panel Standard

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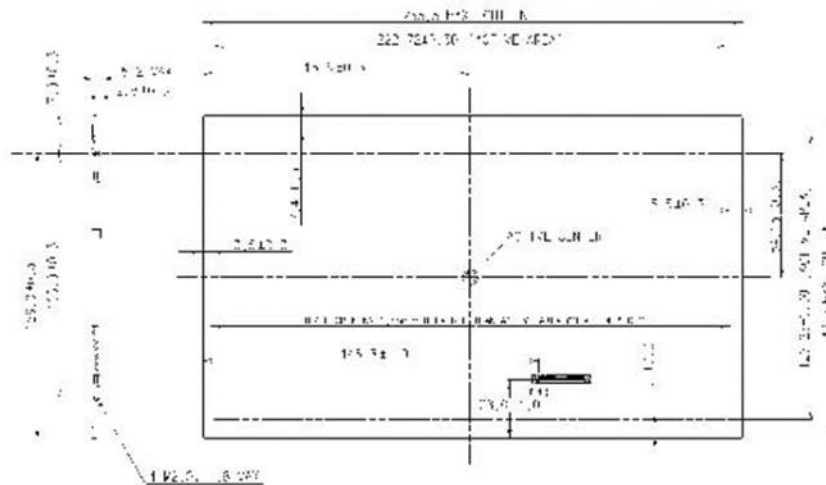
Version 3

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**2.4 Mechanical Interface Requirements**

**2.4.1 10.1-inch Wide 16:9 Panel (LED Backlight Version)**

Figure 2-5 shows the critical exterior dimensions and the location of connectors.



**Figure 2-5: Mechanical Dimensions and Connector Location of 10.1-inch Wide 16:9 LED Panel**

**Notes:**

All dimensions are in mm, and other than side dimensions, are viewed from the front of the panel.

Drawings are not necessarily to scale.

VESA 16:9 Notebook Panel Standard

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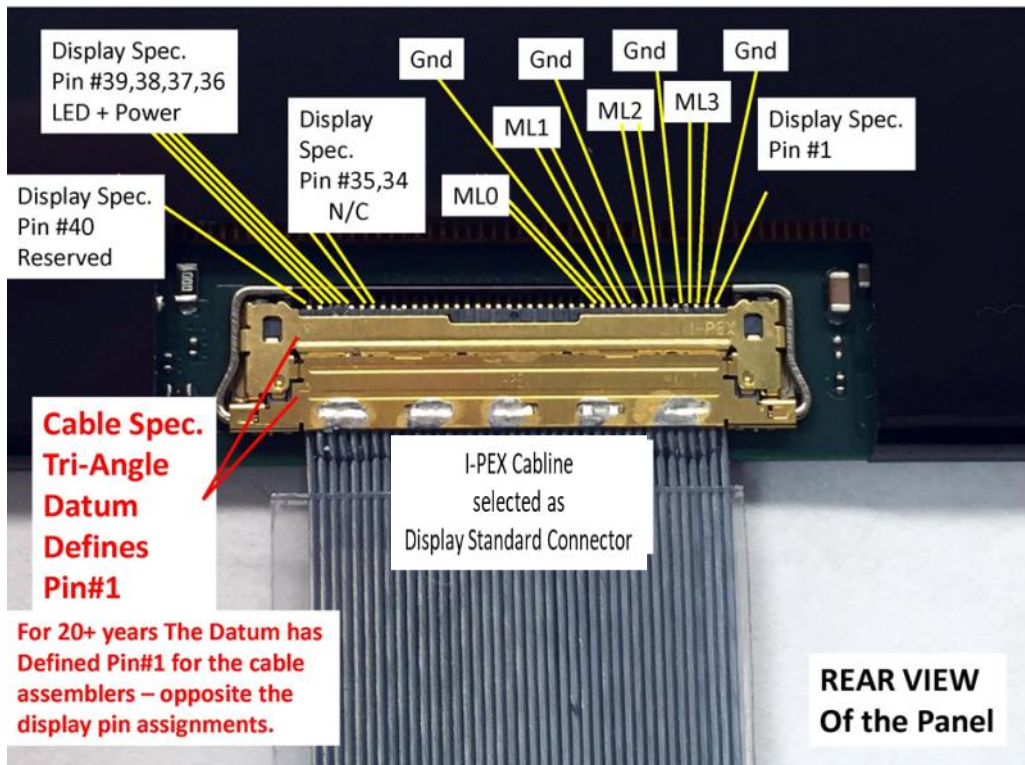
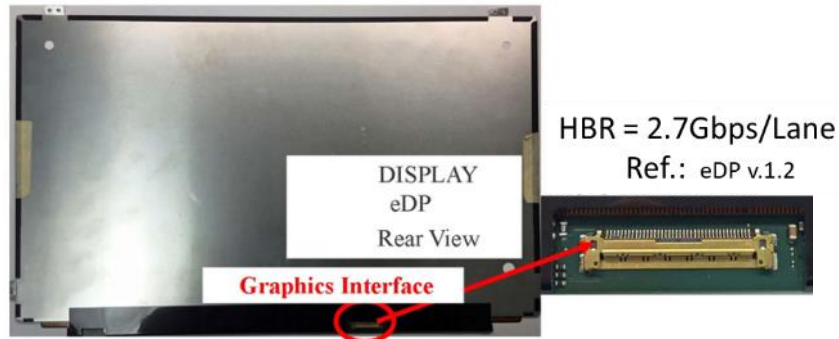




# Pin1 Confusion – Mechanical Specifications Defined from “Front” View of Display Panel

VESA 16:9 Notebook Panel Standard  
LVDS Protocol has different Signal Assignments than eDP™  
Pin1 Nomenclature Confusion remains consistent

## The Display Graphics Connector

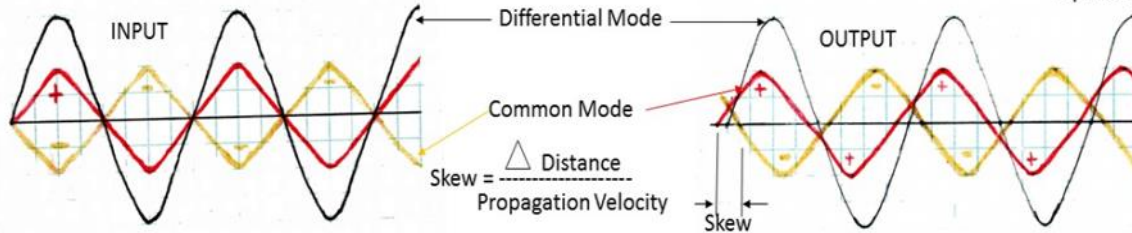
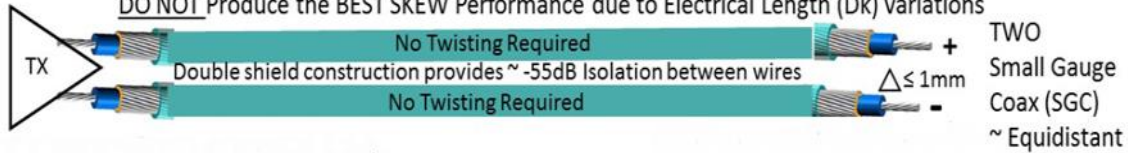


US MaruniTech, Inc (MARUNIX) a Cable Assembly Company will use the **Connector Datum Mark as the Pin 1 designator**

Note: Alternative Cabline Connector Sources I-PEX Licensed TE Connectivity, JAE & others

# “Two SGC” Micro-Coaxial Wires recommended for Differential Signal High Speed Data Transfer

Perfectly/Exact Physical Lengths (+) and (-) are not practical in volume production and **DO NOT** Produce the BEST SKEW Performance due to Electrical Length (Dk) variations



Propagation Velocity changes due to **variation in Insulator Dielectric Constant**

Dk changes with frequency & insulator material properties (Air is the best but not practical)

**SGC**

Usually PFA (Perfluoroalkoxy) Dk ~ 2.1  
PFA Skew < 10ps per meter per lot typical  
Insulation Mid-Point (blue)

**Twin-Coax Construction**

Variation between two insulators  
Non-Flexible types of

**TwinAx Construction**

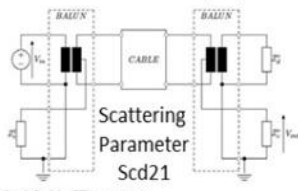
Nonperfect shared Insulator  
RIGID-solid center-conductor

Time Domain Parameters: Skew, Impedance, Eye - Peak Distortion Analysis (PDA) EH & EW  
Scattering Parameters in frequency domain: Insertion Loss (IL)/ ILD, Return Loss (RL), Crosstalk (XTALK), Scd21 Differential conversion

## Balanced SGC Transmission Line to control : Differential to Common Mode Conversion Scd21

Balanced = Equidistant transfer lengths (physically/electrically) & Impedance & Equal Grounding “Symmetry”

At the receiving end, the leakage from the differential-mode to the common mode of a differential lane is called **Transverse Conversion Transfer Loss (TCTL)**.

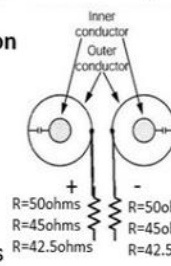
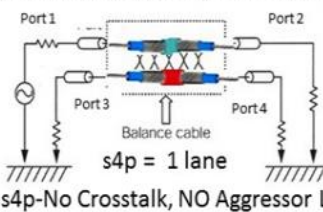


Reference: T. Magesacher

Unbalanced Terminations create EMI issues

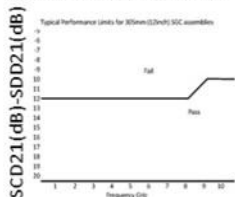
Balanced Terminations With Different Grounding Path Designs: Shield currents take the shortest GND path

### Transverse Electro-Magnetic Propagation



Insulation Thickness Controls Impedance

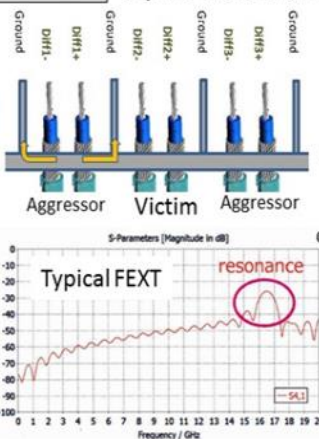
SCD21-SDD21 = Returning differential Signal- The Amplitude SCD21 At Zero Crossing of the Differential Output Causes Differential Skew



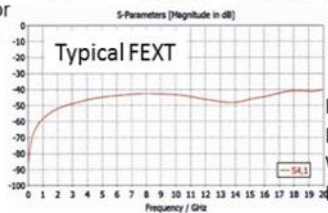
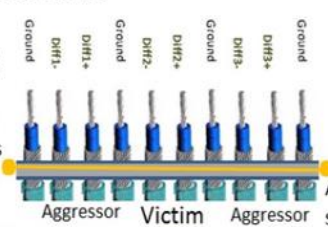
greg\_young@usmarunitech.com

Ground fingers = smaller bundle size & weight for data ≤30Gbps ≤ 15GHz

Shorter GND Path provides Better Low Freq. “RL” Performance for shorter cables

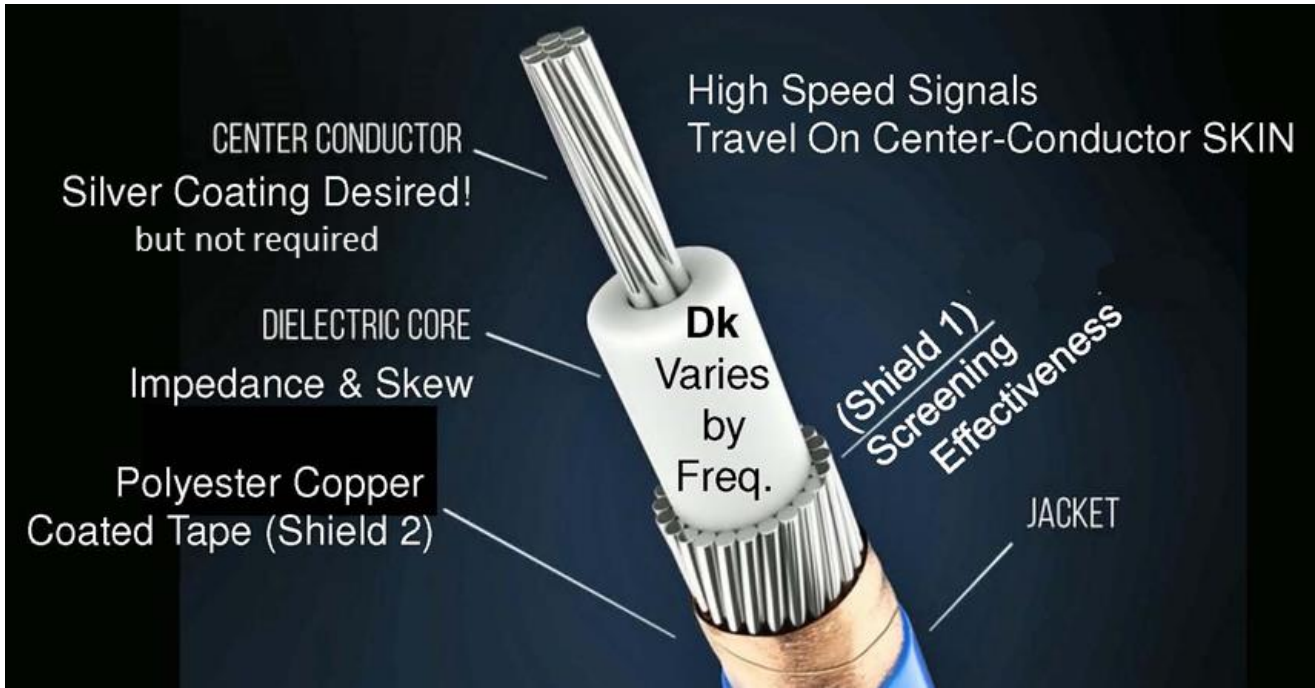


s12p needed for 3 Lane Analysis of 1 Row connector designs

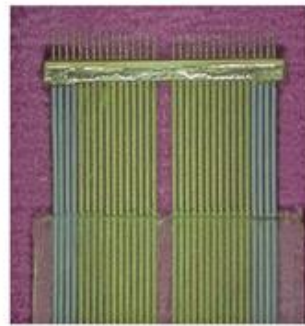
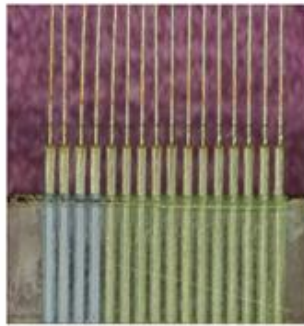
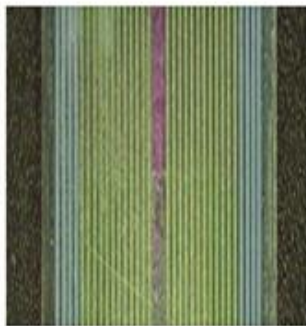


All Coax wire suggested for >30Gbps >15GHz Nyq.  
Long Ground Paths = Worse RL @ Low Freq.





### Harness assembly processes (solder connector)



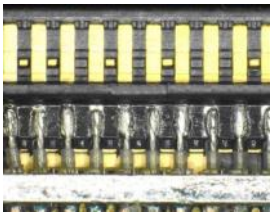
Lasers = low labor assembly process



Cables in line according to connector pitch

Cut cables (jacket/shield/insulation) using laser

Solder shield using ground bar



Solder connector and inner conductor

After installing shell, solder shell and ground bar

Foam and tape if needed



# eDP™

## DisplayPort Data Rates:

HBR = 2.7 Gbps per Lane = Nyquist Frequency 1.35 GHz

HBR2 = 5.4Gbps per Lane = Nyquist Frequency 2.7 GHz

HBR3 = 8.1Gbps per Lane = Nyquist Frequency 4.05 GHz

Note: HBR was released during 2010

## In Development

- UHBR10 Lane Data Rates to 10Gbps = Nyquist Frequency 5.0 GHz
- UHBR20 Lane Data Rates to 20 Gbps = Nyquist Frequency 10 GHz

## Example eDP Panel Connector Pinout

### 2 Lane eDP Connector for up to 1920 x 1080 60Hz

Conn. Pin	Pin	Signal Name	Description
30	1	NC - RESERVED	RESERVED for LCD manufacturer's use
29	2	H_GND	High Speed Ground
28	3	Lane1_N	Complement Signal Link Lane 1
27	4	Lane1_P	True Signal Link Lane 1
26	5	H_GND	High Speed Ground
25	6	Lane0_N	Complement Signal Link Lane 0
24	7	Lane0_P	True Signal Link Lane 0
23	8	H_GND	High Speed Ground
22	9	AUX_CH_P	True Signal Auxiliary Channel
21	10	AUX_CH_N	Complement Signal Auxiliary Channel
20	11	H_GND	High Speed Ground
19	12	LCD_VCC	LCD logic and driver power
18	13	LCD_VCC	LCD logic and driver power
17	14	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
16	15	LCD_GND	LCD logic and driver ground
15	16	LCD_GND	LCD logic and driver ground
14	17	HPD	HPD signal pin
13	18	BL_GND	Backlight ground
12	19	BL_GND	Backlight ground
11	20	BL_GND	Backlight ground
10	21	BL_GND	Backlight ground
09	22	BL_ENABLE or NC	Backlight On/Off (Optional)
08	23	BL_PWM_DIM or NC	System PWM signal input for dimming (optional)
07	24	NC - Reserved	Reserved for LCD manufacturer's use
06	25	NC - Reserved	Reserved for LCD manufacturer's use
05	26	BL_PWR	Backlight power
04	27	BL_PWR	Backlight power
03	28	BL_PWR	Backlight power
02	29	BL_PWR	Backlight power
01	30	NC - RESERVED	RESERVED for LCD manufacturer's use

Optional, depending on display resolution

Signal Pins

Main Link Lanes  
(Display data)

AUX Channel  
(Control data)

Hot Plug Detect  
(AUX interrupt)

Power and Ground Pins

Display Control Pins  
(Now optional with eDP v1.2)

Reserved Pins  
(For LCD OEM's use)

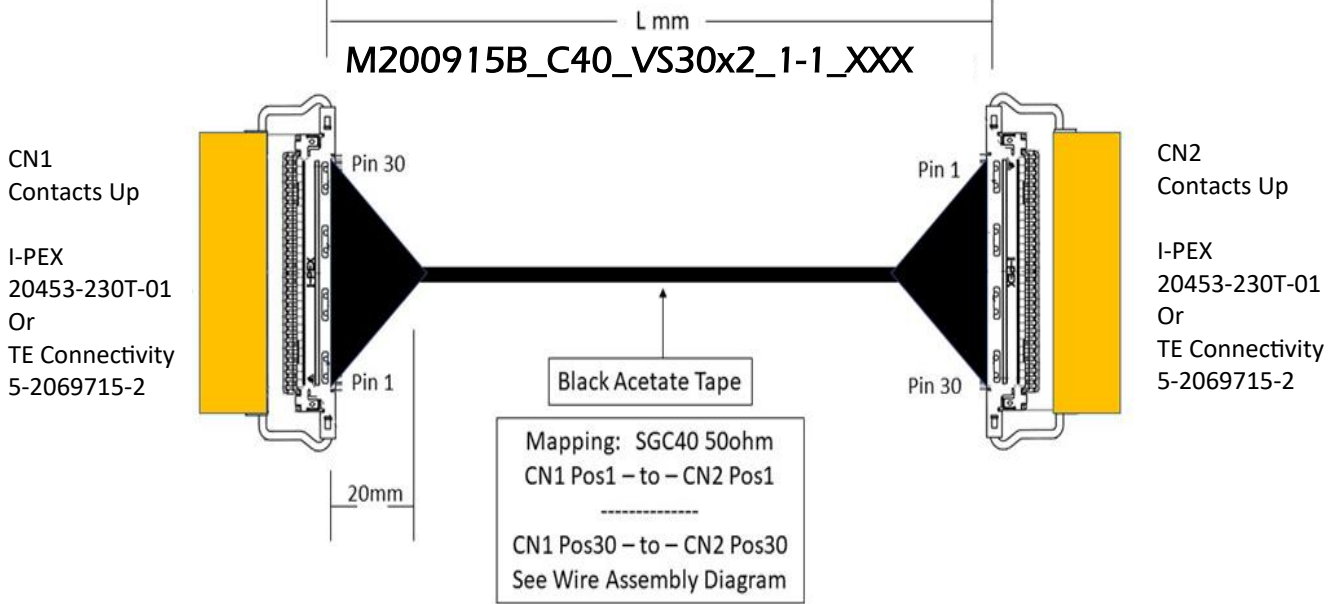


Table 5-3 in eDP v1.2

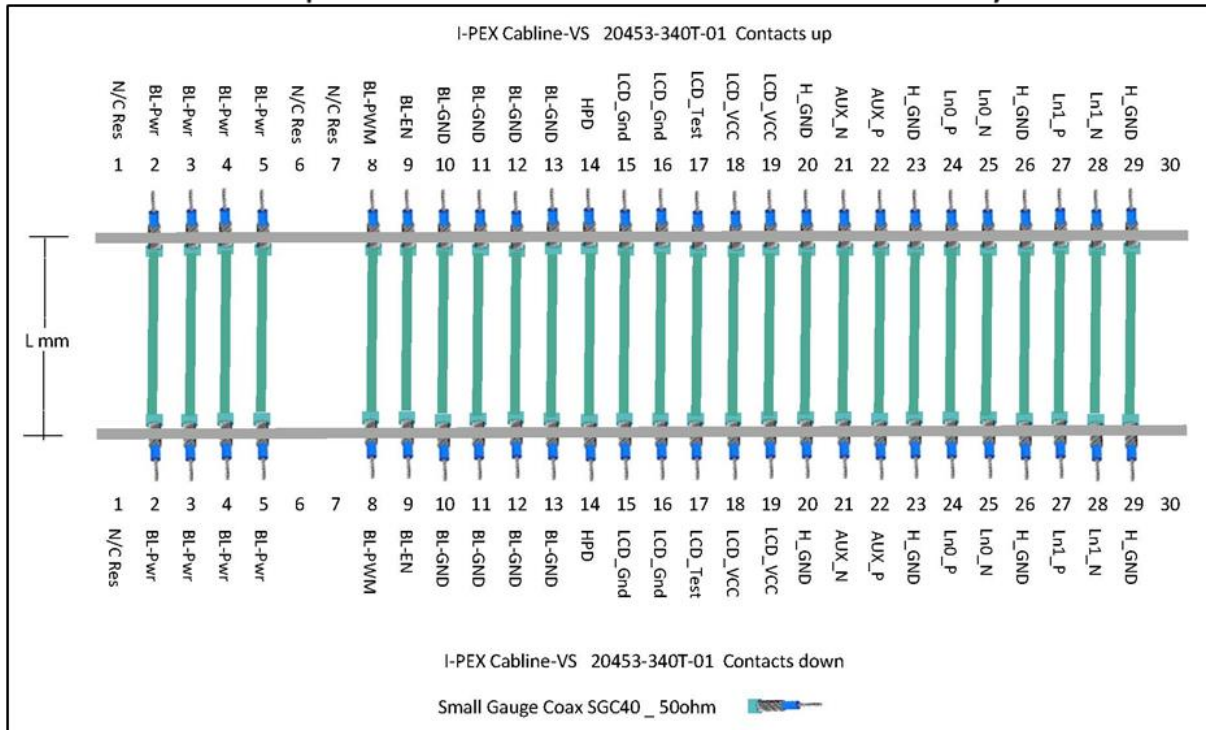




DISPLAY CABLE ASSEMBLY VS30p BUNDLED STANDARD



30p 2 Lane eDP Standard Wire Assembly



Bundle Formula

$$(D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i})$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

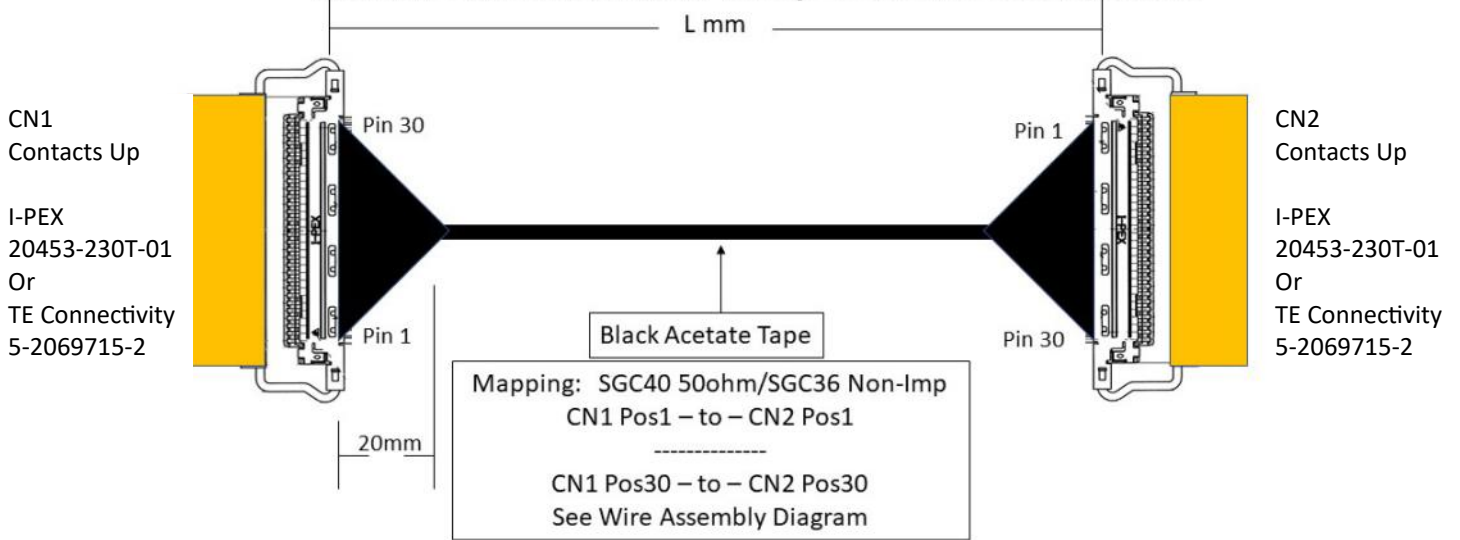
SGC40 50ohm =  $\varnothing 0.36 \pm 0.02$ mm  
 Center Conductor Resistance = 5  $\Omega$ /m  
 D =  $\varnothing 2.33$  mm  
 Est. 180deg. Bending Radius = ~11.6 mm



Bundled Construction 1-1 signal mapping & Wire Assembly Options

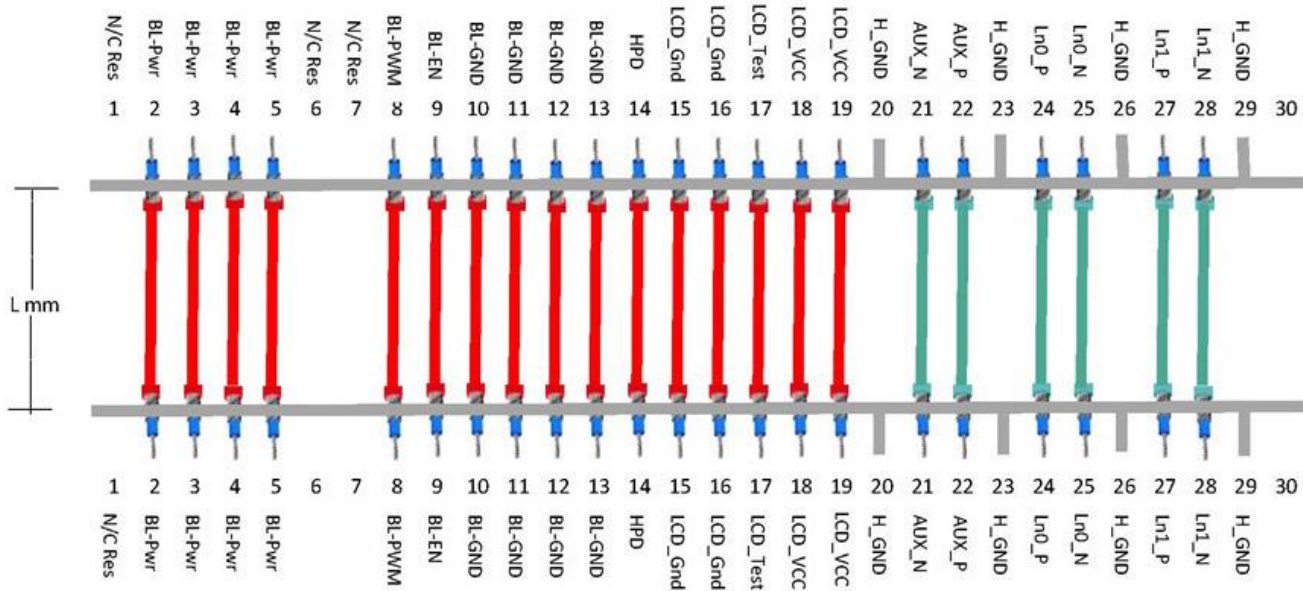
M200915B\_C40-36\_VS30x2\_1-1\_XXX

DISPLAY CABLE ASSEMBLY VS30p BUNDLED SGC40/SGC36



M200915\_B\_C40-36\_VS30x2\_1-1\_XXX wire assembly

I-PEX Cabline-VS 20453-230T-01 Contacts Up



I-PEX Cabline-VS 20453-230T-01 Contacts Down

Small Gauge Coax SGC36  
Non-Controlled Impedance Signals  
Center Conductor Resistance: 1.5 ohms/m

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance Signals

Bundle Formula

$$D = \sqrt{[\sum d_i^2] + \sum \Delta t_i}$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

SGC40 50ohm =  $\varnothing 0.36 \pm 0.02$ mm

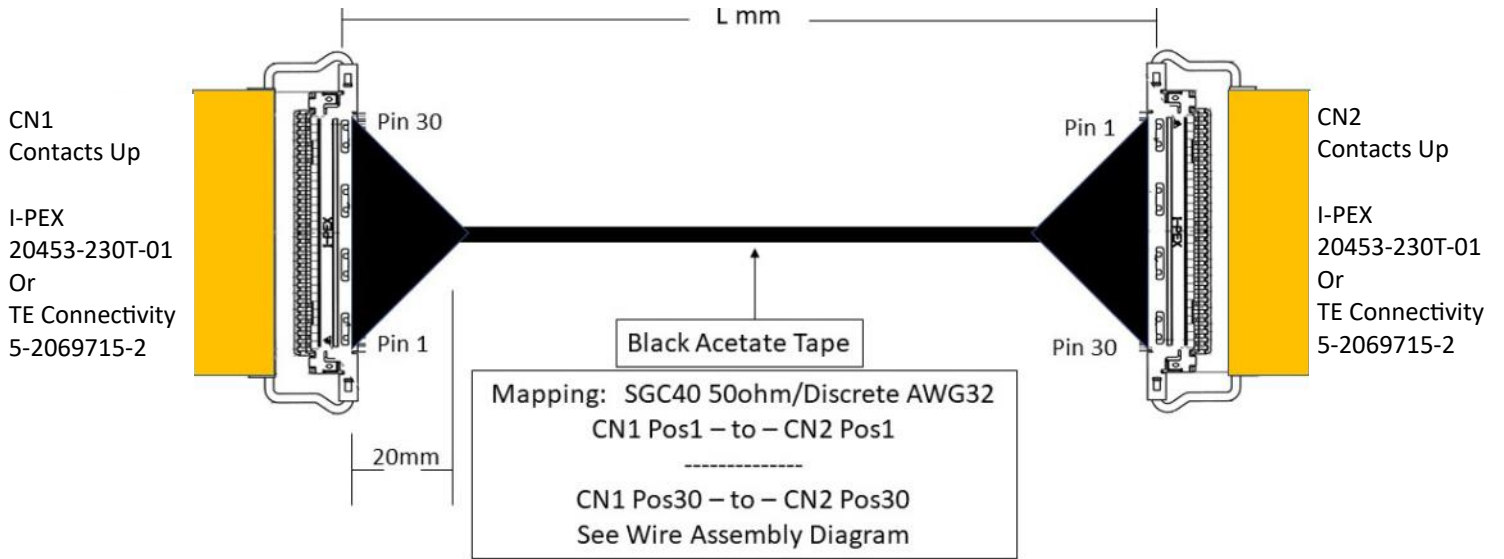
SGC36 Non-Imp Controlled =  $\varnothing 0.365 \pm 0.02$ mm

D =  $\varnothing 2.16$  mm

Est. 180deg. Bending Radius =  $\sim 10.8$  mm

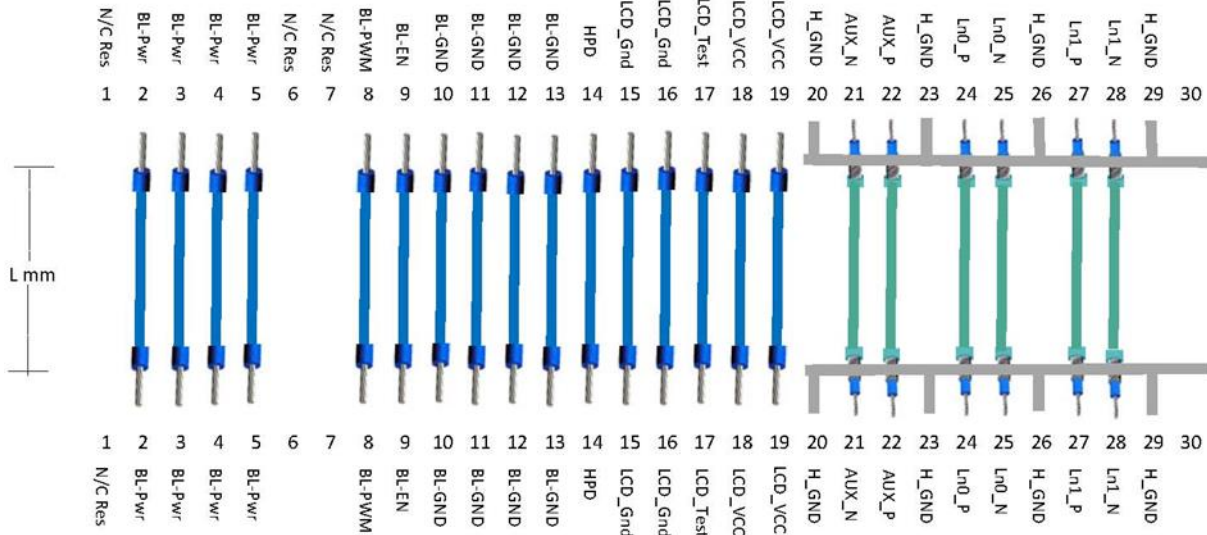
Bundled Construction 1-1 signal mapping & Wire Assembly Options

M200915B\_C40-D32\_VS30x2\_1-1\_XXX



30p 2 Lane eDP SGC40 Gnd-Finger/D32 Mixed Wire Assembly

I-PEX Cabline-VS 20453-240T-01 Contacts Up



I-PEX Cabline-VS 20453-240T-01 Contacts Down

UL 10064 Discrete AWG32  
Center Conductor Resistance: 0.6 Ω/m

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance Signals

Bundle Formula

$$(D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i})$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

SGC40 50ohm =  $\varnothing 0.36 \pm 0.02$ mm

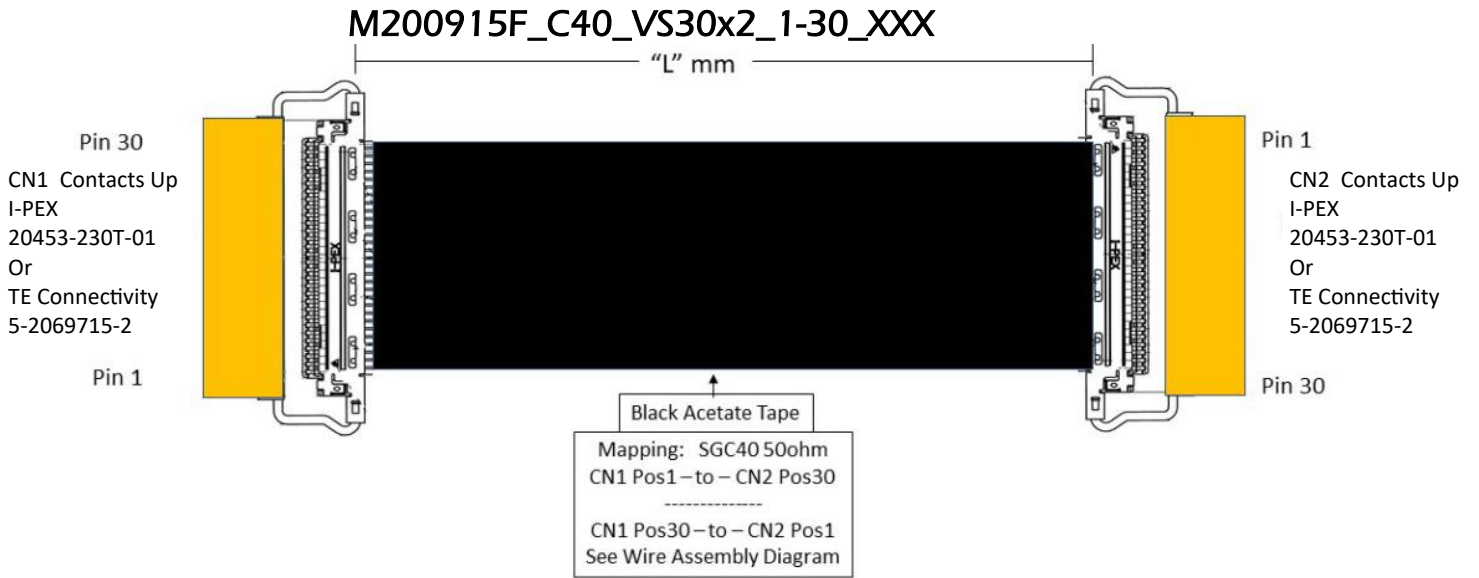
Discrete D32 =  $\varnothing 0.38 \pm 0.03$ mm

D =  $\varnothing 2.26$  mm (no tape included)

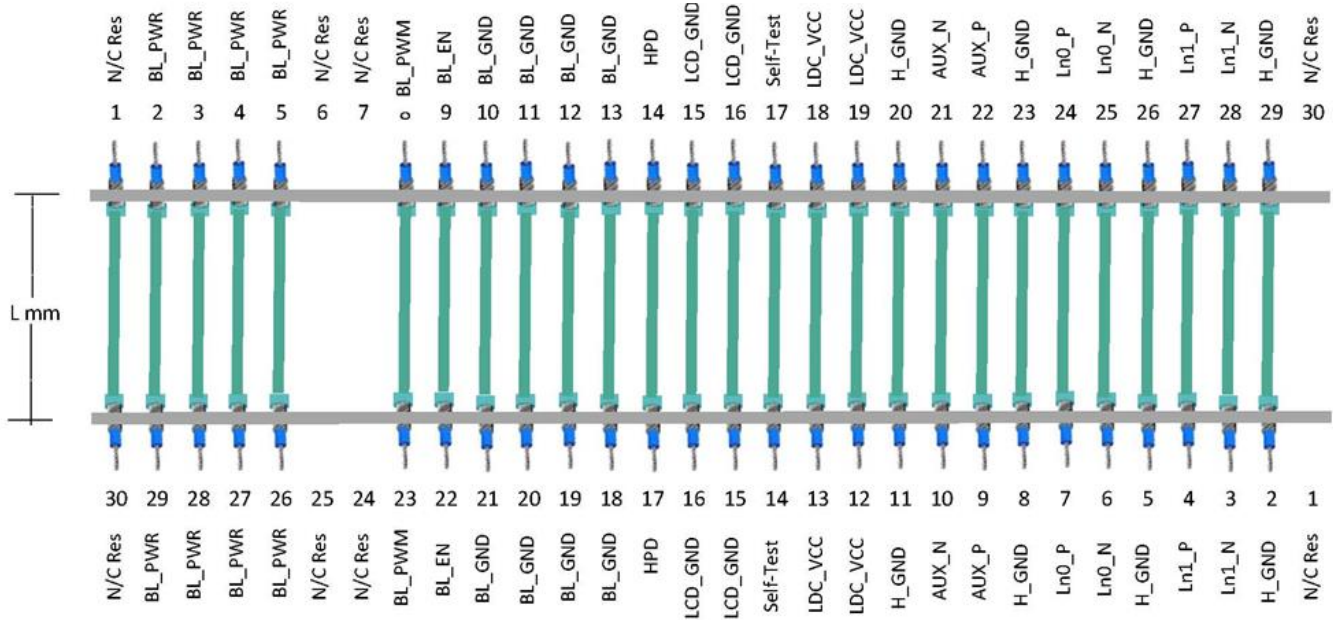
Est. 180deg. Bending Radius =  $\sim 11.3$  mm



# 30p 2-Lane eDP Display Cable Assembly 1-30 Flat Ribbon Type




## Cablne-VS 20453-230T-01 Contacts Up



## Cablne-VS 20453-230T-01 Contacts Up

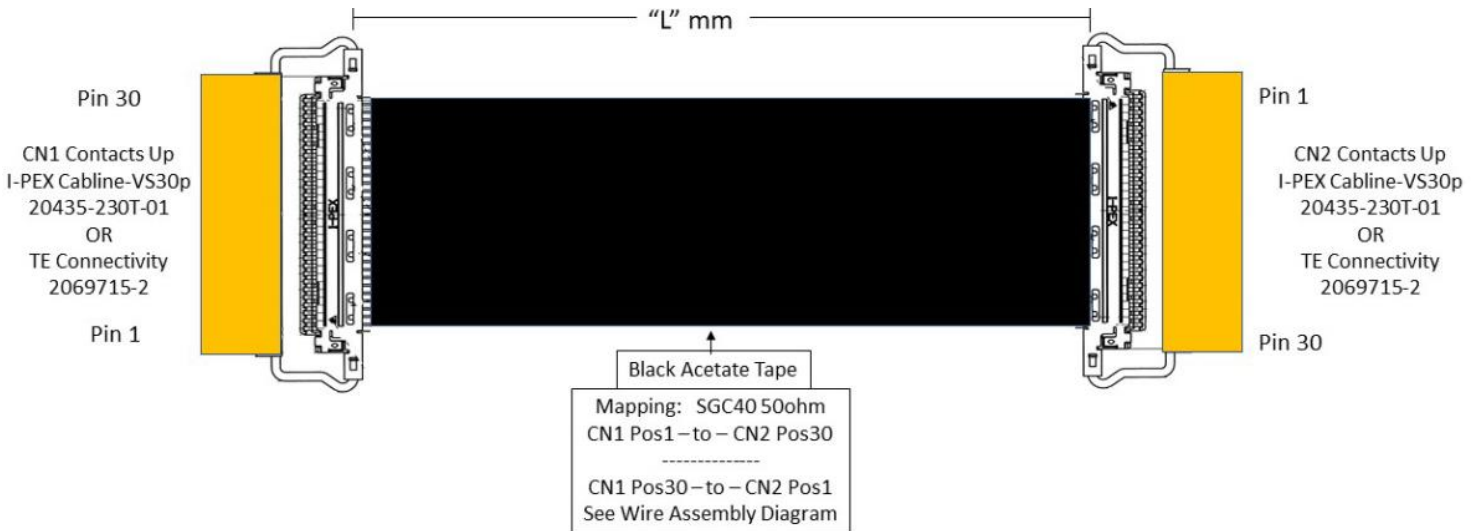
Small Gauge Coax SGC40\_50ohm  
Controlled Impedance



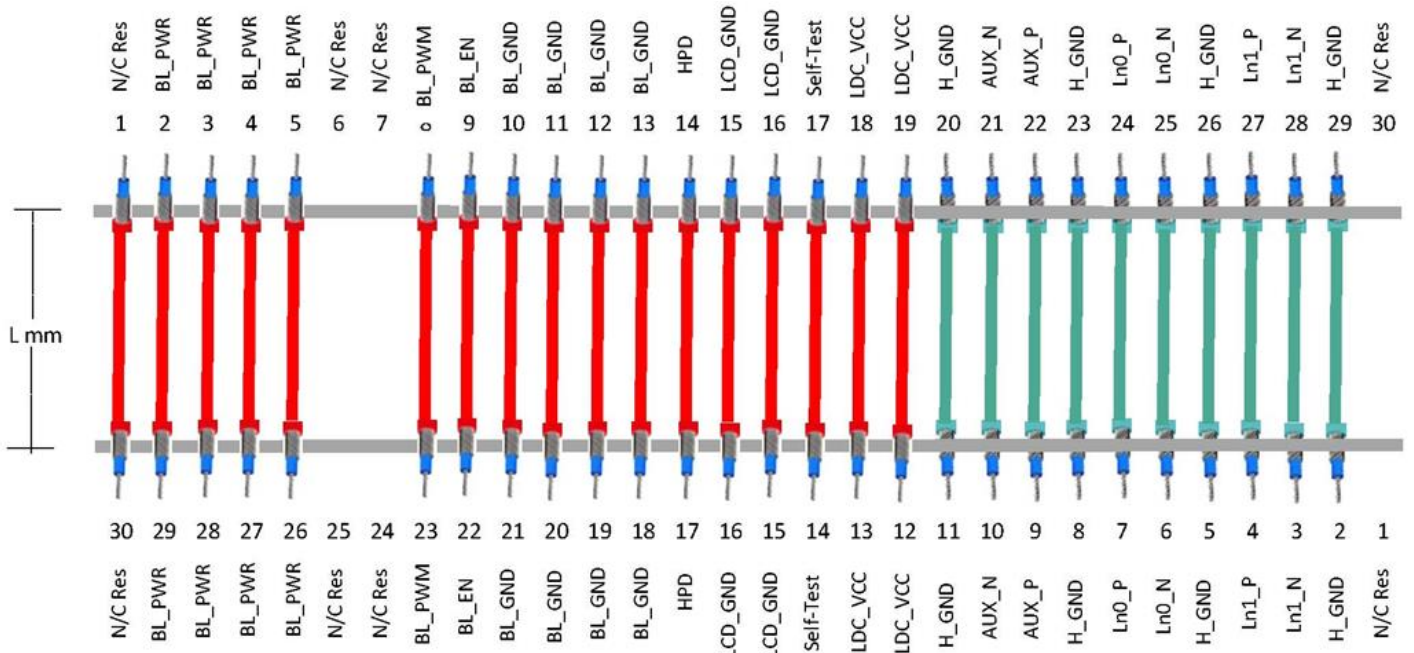
For Power signals: SGC40 Center Conductor Resistance = 5 Ω/m  
180 deg. Bending Radius = ~ 2.4mm




M200915F\_C40-36\_VS30x2\_1-30\_XXX




**Cabline-VS 20453-230T-01 Contacts Up**



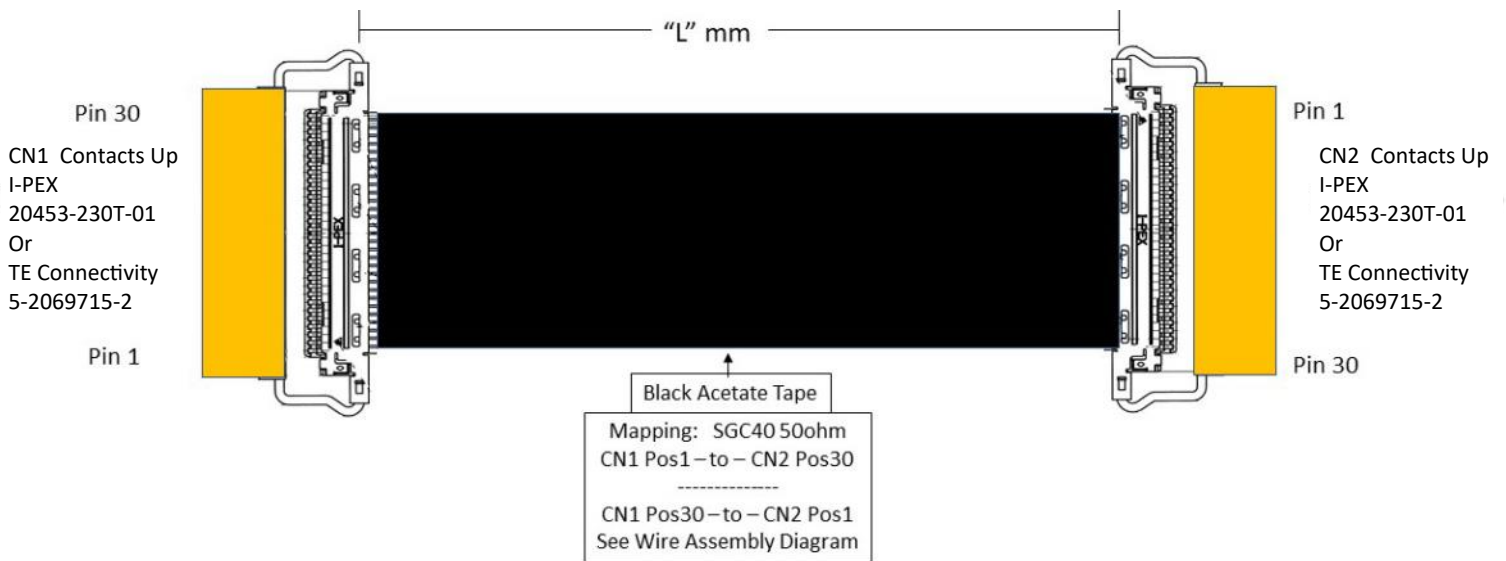
**Cabline-VS 20453-230T-01 Contacts Up**

Small Gauge Coax SGC36   
 For NON-Controlled Impedance Signals  
 Center conductor Resistance = 1.5 Ω/m

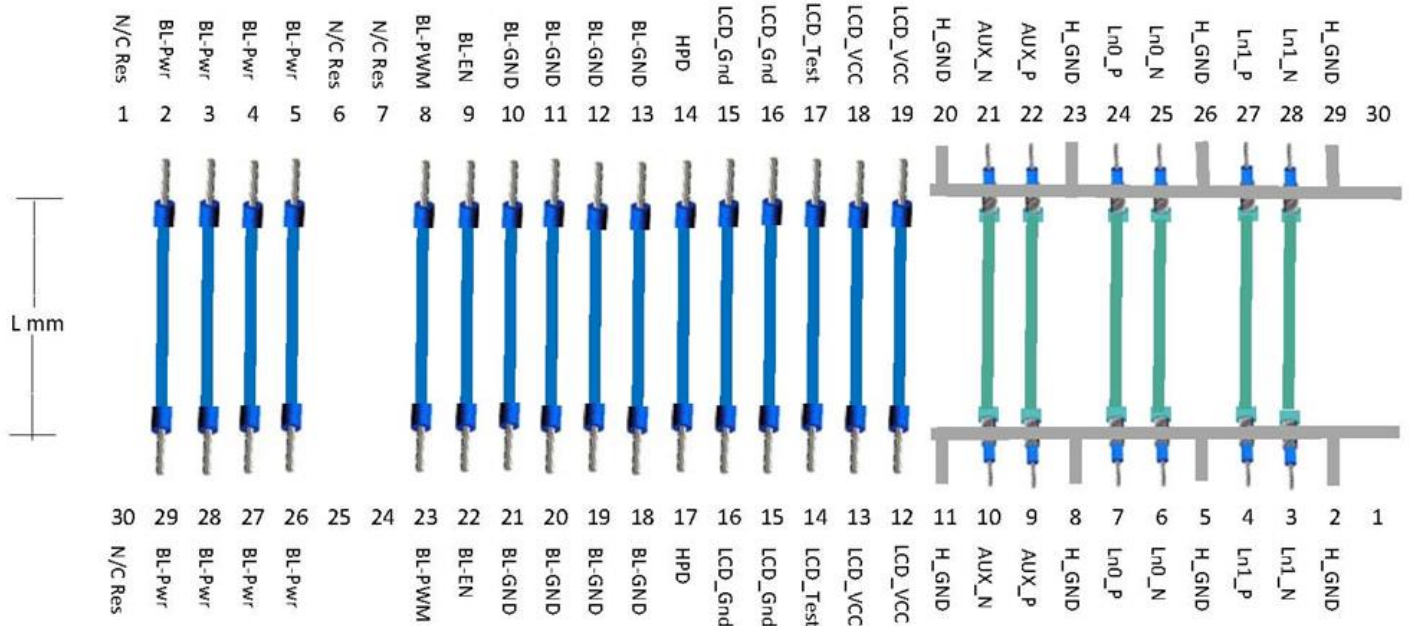
Small Gauge Coax SGC40\_50ohm   
 Controlled Impedance Signals

For Power signals: SGC36 Center Conductor Resistance = 1.5 Ω/m  
 180 deg. Bending Radius = ~ 2.53mm

M20915F\_C40-D32\_VS30x2\_1-30\_XXX



Cablne-VS 20453-230T-01 Contacts Up



Cablne-VS 20453-230T-01 Contacts Up

UL 10064 Discrete AWG32  
Center Conductor Resistance: 0.6 Ω/m

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance Signals

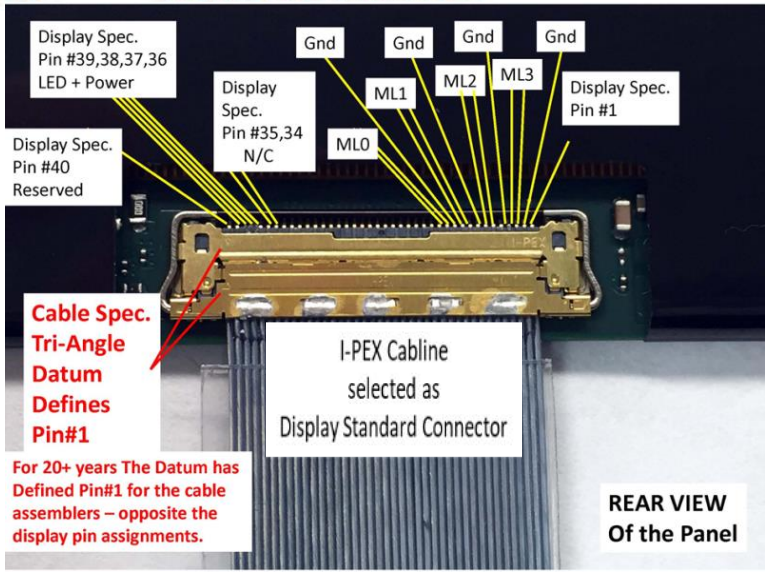
For Power signals: D32 Center Conductor Resistance = 0.6 Ω/m  
180 deg. Bending Radius = ~2.53 mm



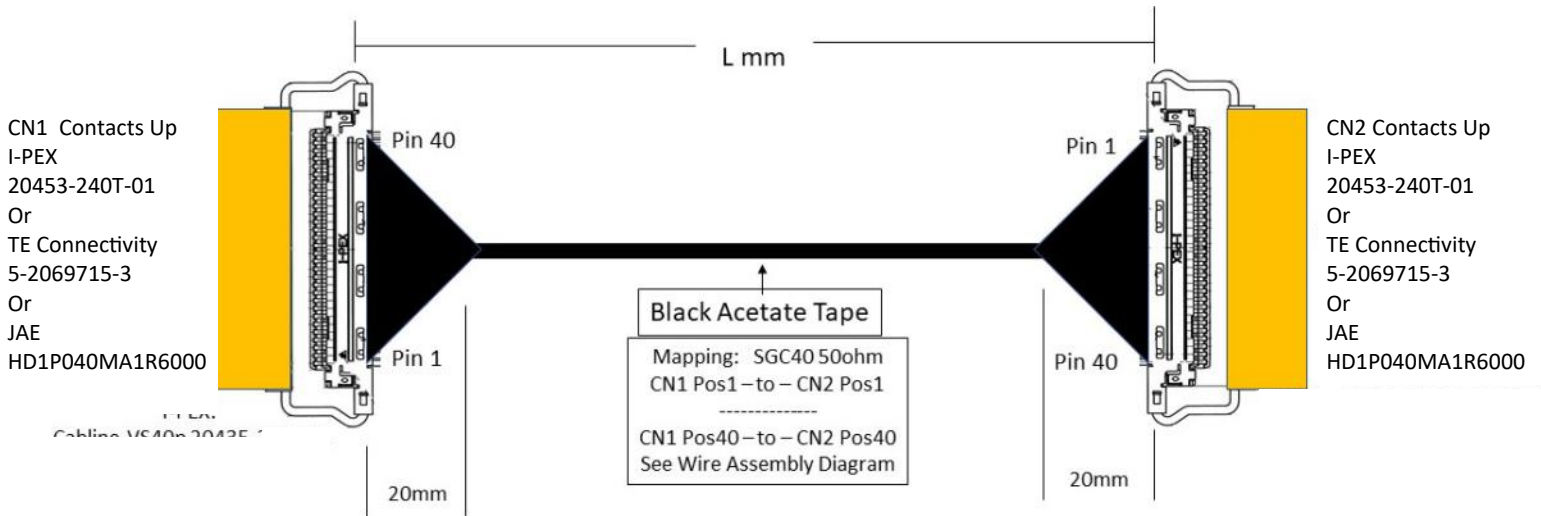


Display Pin Position	Signal Name	Description
40	1	N/C Reserved
39	2	H_Gnd
38	3	Lane3_N
37	4	Lane3_P
36	5	H_Gnd
35	6	Lane2_N
34	7	Lane2_P
33	8	H_Gnd
32	9	Lane1_N
31	10	Lane1_P
30	11	H_Gnd
29	12	Lane0_N
28	13	Lane0_P
27	14	H_Gnd
26	15	AUX_CH_P
25	16	AUX_CH_N
24	17	H_Gnd
23	18	LCD_VCC
22	19	LCD_VCC
21	20	LCD_VCC
20	21	LCD_VCC
19	22	LCD_Self_Test or NC
18	23	LCD_GND Return
17	24	LCD_GND Return
16	25	LCD_GND Return
15	26	LCD_GND Return
14	27	HPD
13	28	BL_GND
12	29	BL_GND
11	30	BL_GND
10	31	BL_GND
9	32	BL_ENABLE or NC
8	33	BL_PWM_DIM or NC
7	34	NC - Reserved
6	35	NC - Reserved
5	36	BL_PWR
4	37	BL_PWR
3	38	BL_PWR
2	39	BL_PWR
1	40	NC - Reserved

Conn Pin

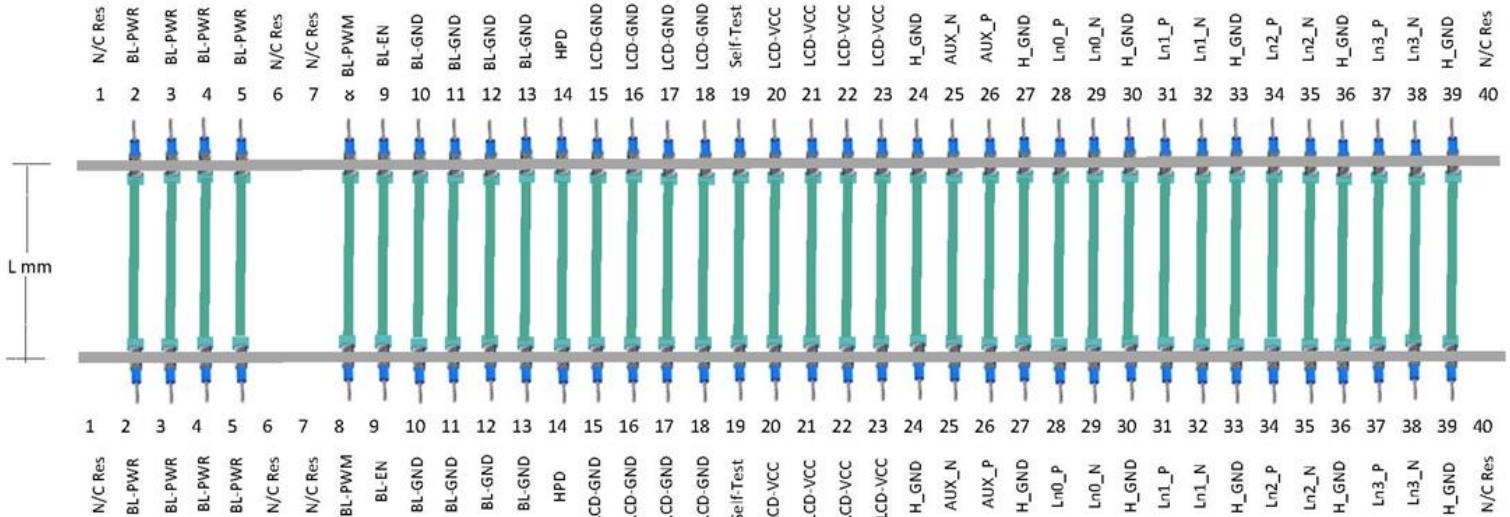


M200915B\_C40\_VS40x2\_1-1\_XXX



WIRE Assembly

I-PEX Cabline-VS 20453-240T-01 Contacts UP



I-PEX Cabline-VS 20453-240T-01 Contacts DOWN

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance  
Center Conductor Resistance = 5 Ω/m

Bundle Formula

$$D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i}$$

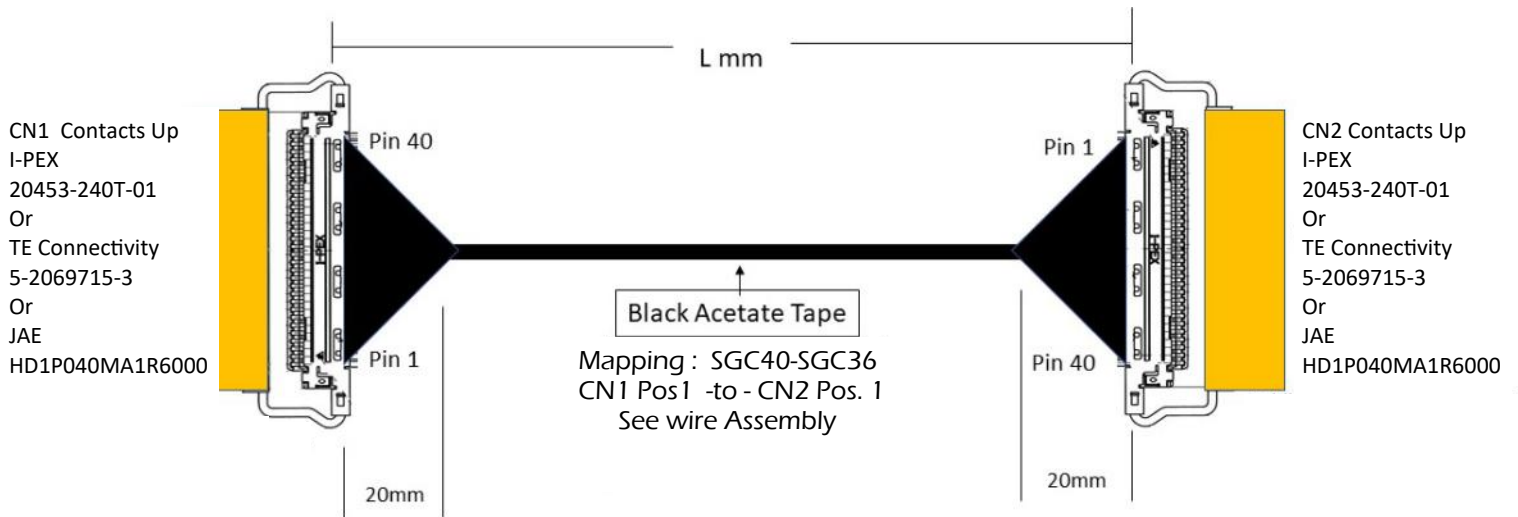
$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

SGC40 50ohm =  $\varnothing 0.36 \pm 0.02$ mm  
Center Conductor Resistance = 5 Ω/m  
D =  $\varnothing 2.86$  mm  
Est. 180deg. Bending Radius = ~14.3 mm



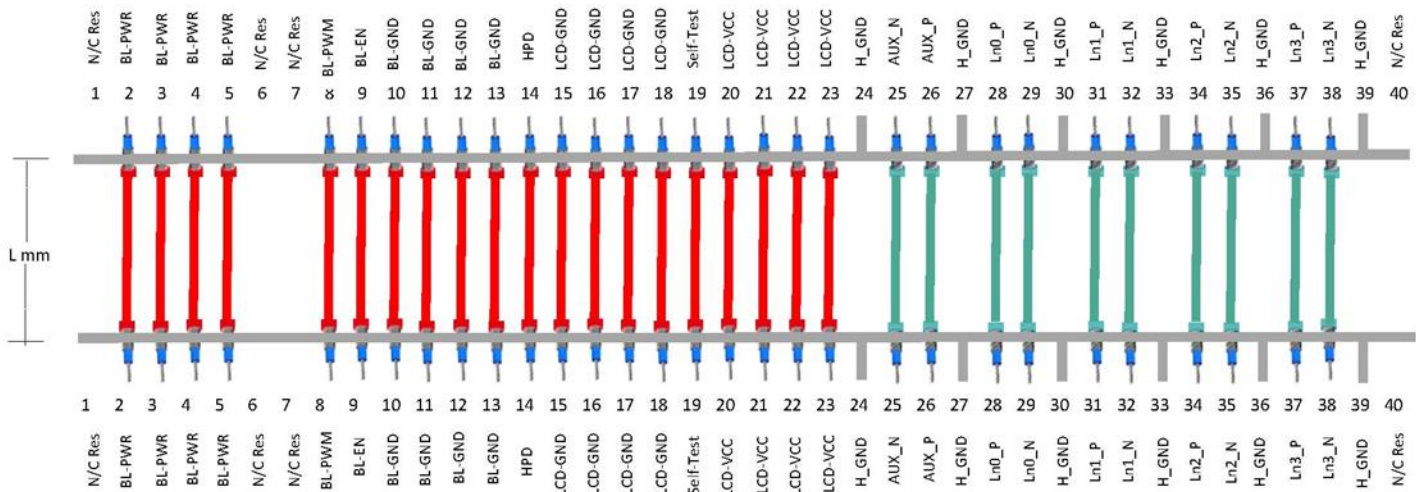
### OPTIMUM Wire Assembly Design

M200915B\_C40-36\_VS40x2\_1-1\_xxx



### WIRE Assembly

I-PEX Cabline-VS 20453-240T-01 Contacts UP



I-PEX Cabline-VS 20453-240T-01 Contacts DOWN

I-PEX Cabline-VS 20453-240T-01 Contacts DOWN

Small Gauge Coax SGC36  
NON-Controlled Impedance Signals  
Center Conductor Resistance = 1.5 Ω/m

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance Signals

### Bundle Formula

$$D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i}$$

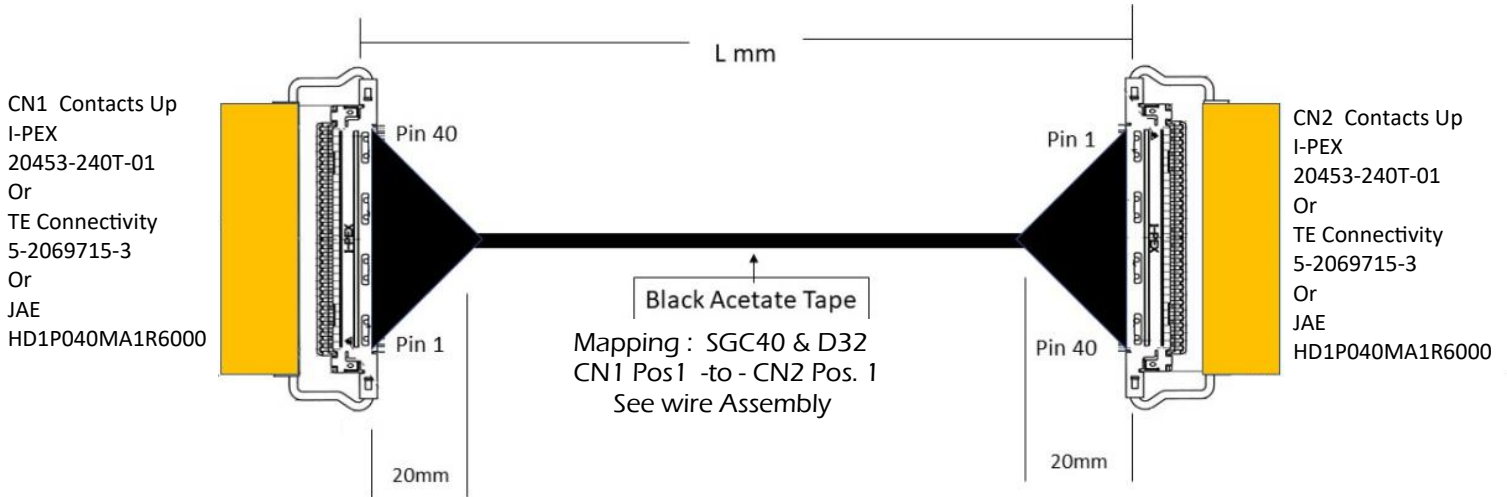
$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

SGC40 50ohm =  $\varnothing 0.36 \pm 0.02$ mm  
 SGC36 Non-Imp =  $\varnothing 0.365 \pm 0.02$ mm  
 D =  $\varnothing 2.63$  mm  
 Est. 180deg. Bending Radius =  $\sim 13.2$  mm



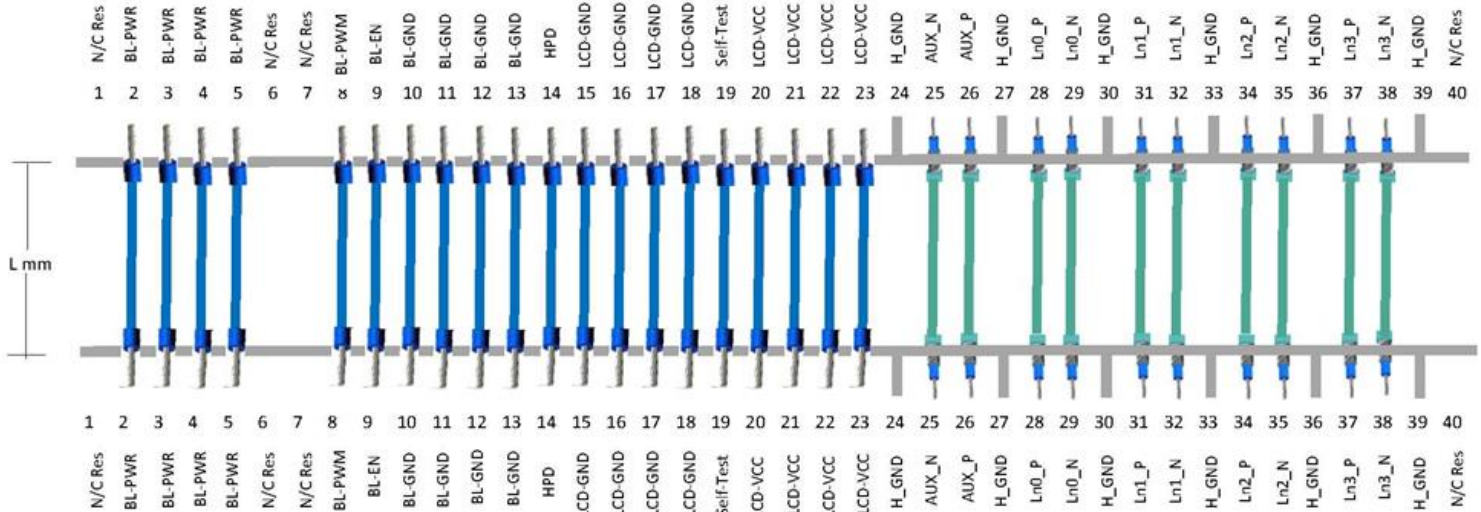
Mixed Coax & Discrete Wire Assembly

M200915B\_C40-D32\_VS40x2\_1-1\_XXX



WIRE Assembly

I-PEX Cabline-VS 20453-240T-01 Contacts UP



I-PEX Cabline-VS 20453-240T-01 Contacts Down

UL 10064 Discrete AWG32  
Center Conductor Resistance = 0.6 Ω/m

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance Signals

Bundle Formula

$$D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i}$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

SGC40 50ohm =  $\varnothing 0.36 \pm 0.02$ mm

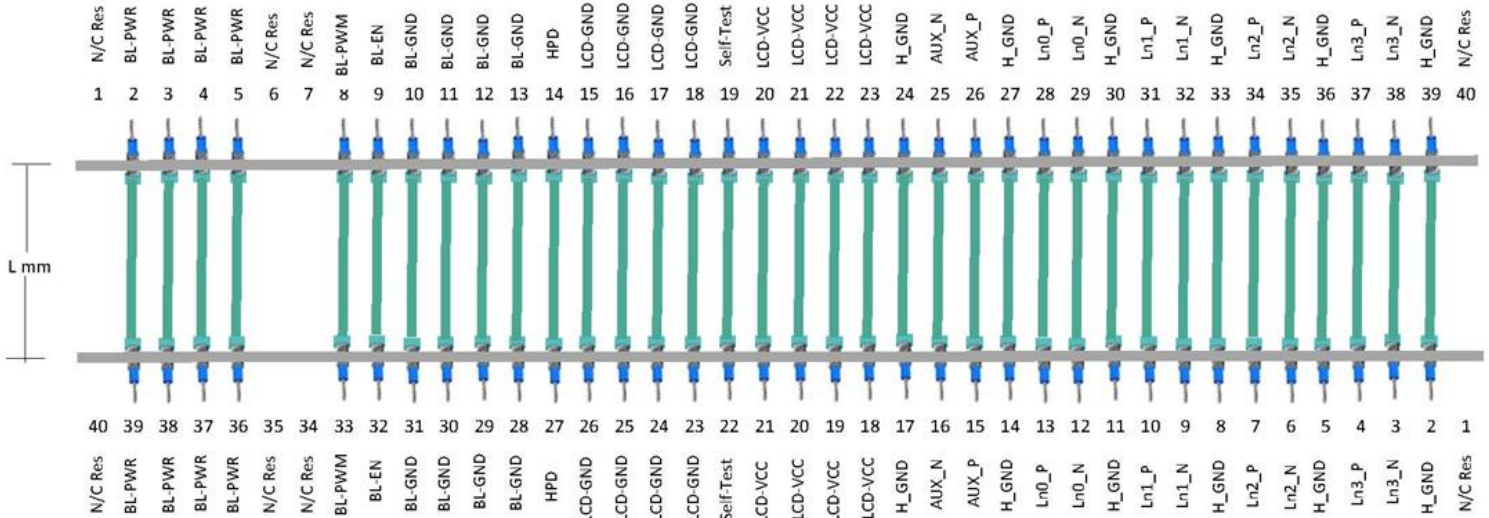
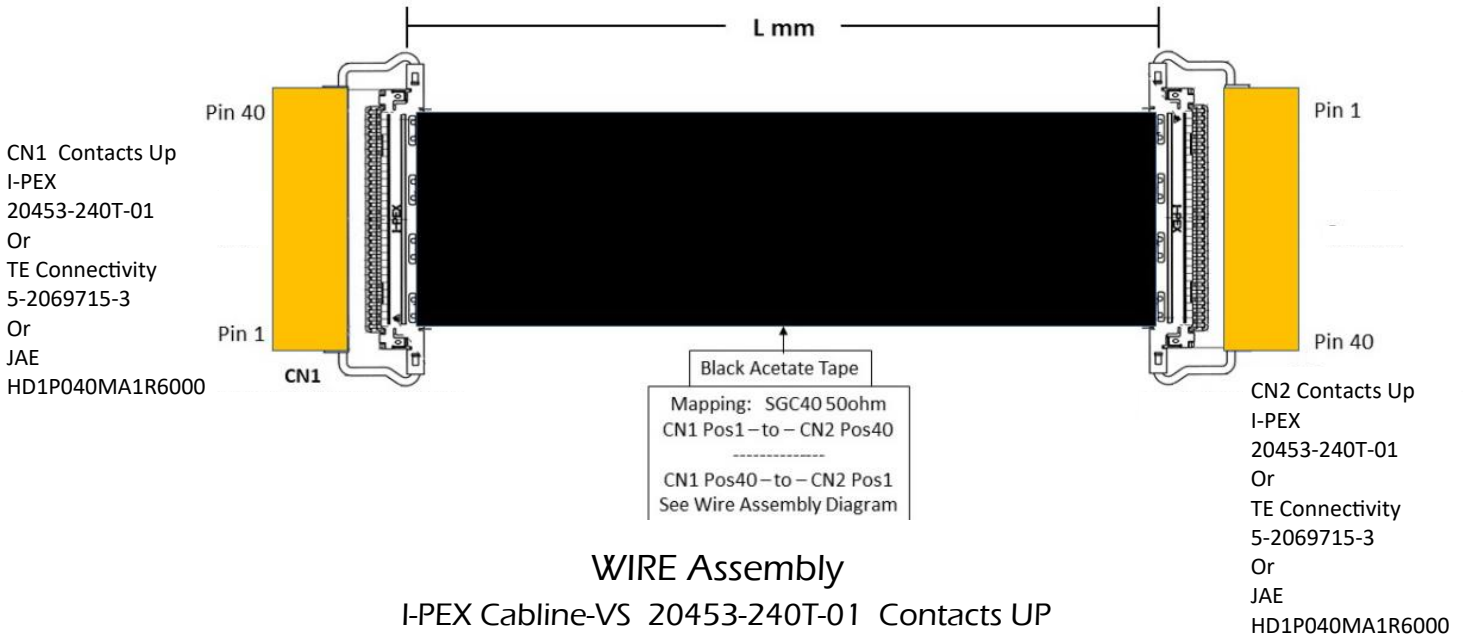
D32 =  $\varnothing 0.38 \pm 0.03$ mm

D =  $\varnothing 2.75$  mm


Est. 180deg. Bending Radius = ~13.75 mm

For Power signals: D32 Center Conductor Resistance = 0.6 Ω/m

M200915F\_C40\_VS40x2\_1-40\_xxx



I-PEX Cabline-VS 20453-240T-01 Contacts UP

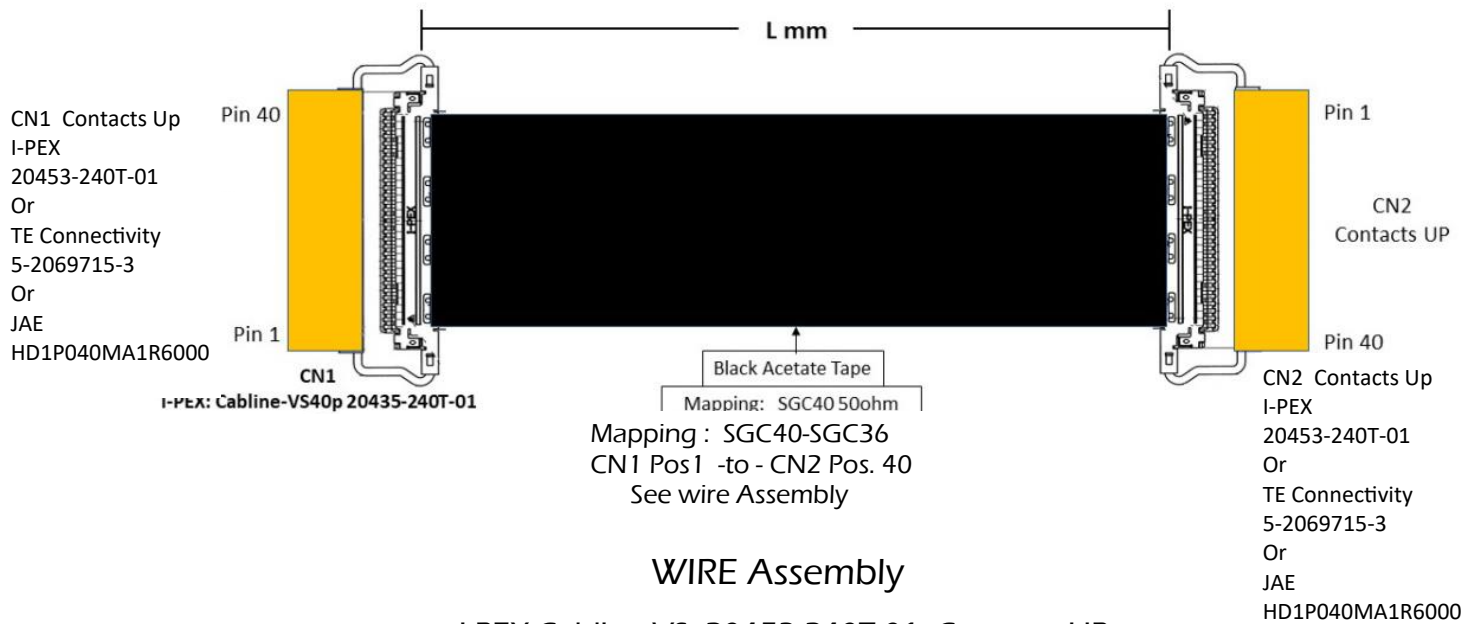
Small Gauge Coax SGC40\_50ohm   
Controlled Impedance  
Center Conductor Resistance = 5 Ω/m

For Power signals: SGC40 Center Conductor Resistance = 5 Ω/m  
180 deg. Bending Radius = ~ 2.5mm



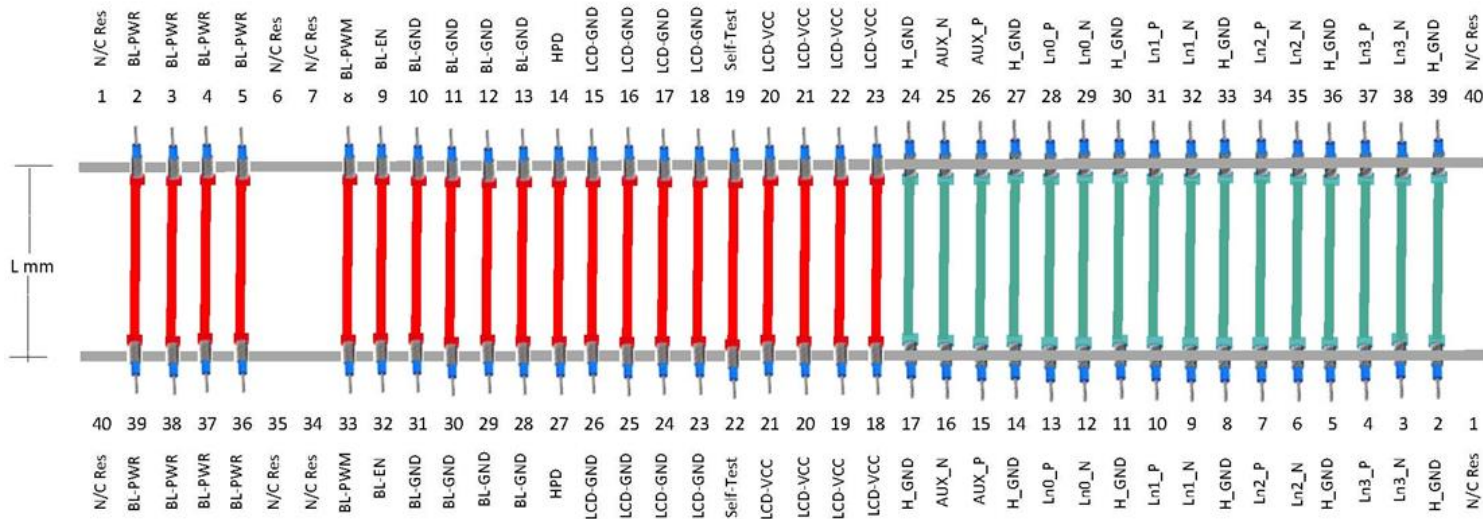
OPTIMUM Wire Assembly Design

M200915F\_C40-36\_VS40x2\_1-40\_XXX



WIRE Assembly

I-PEX Cabline-VS 20453-240T-01 Contacts UP



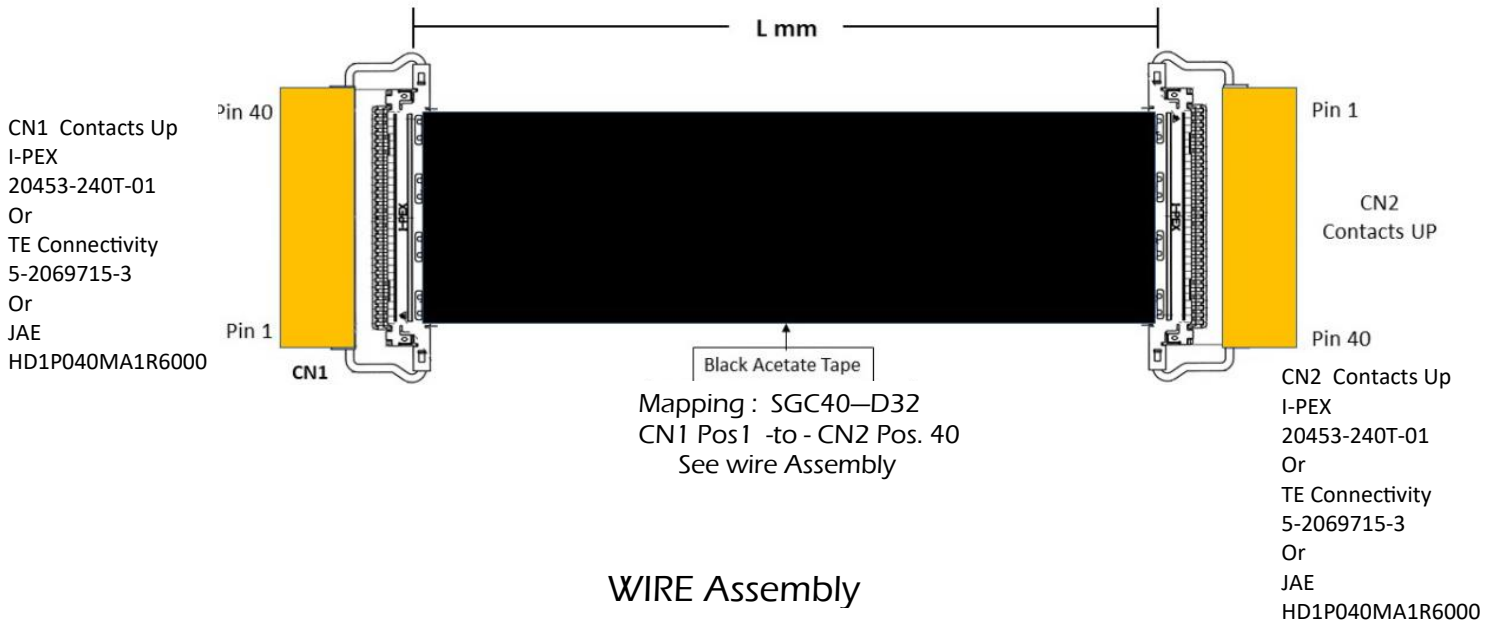
I-PEX Cabline-VS 20453-240T-01 Contacts UP



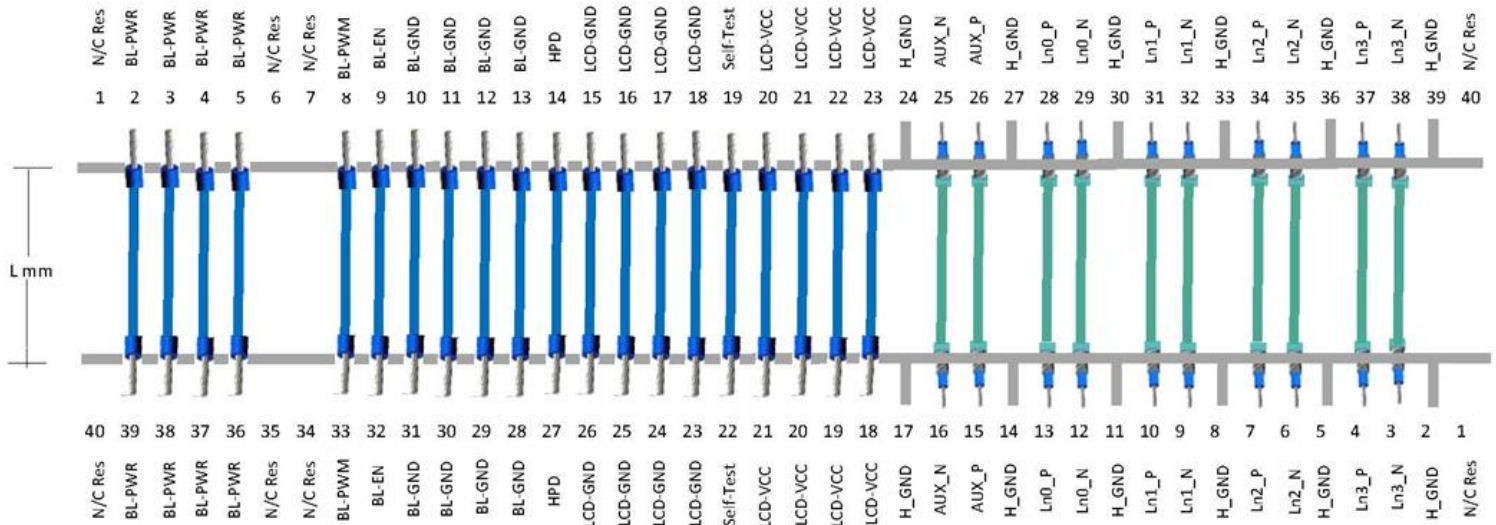
For Power signals: SGC36 (Non-Imp) Center Conductor Resistance = 1.5 Ω/m  
 180 deg. Bending Radius = ~ 2.53 mm



M200915F\_C40-D32\_VS40x2\_1-40\_xxx



I-PEX Cabline-VS 20453-240T-01 Contacts UP



I-PEX Cabline-VS 20453-240T-01 Contacts UP

UL 10064 Discrete AWG32  
Center Conductor Resistance = 0.6 Ω/m

Small Gauge Coax SGC40\_ 50ohm  
Controlled Impedance Signals

For Power signals: D32 Center Conductor Resistance = 0.6 Ω/m  
180 deg. Bending Radius = ~ 2.65 mm





## VESA 16:9 Wide Notebook Panel Standard

Version 3

9 November 2010

### Purpose

This standard defines the requirements for the standardization of mechanical dimensions and selected electrical interface requirements for 10.1-, 11.6-, 13.3-, 13.4-, 14.0-, 15.6-, 17.3- and 18.4-inch W (wide format) 16:9 panels. The intent of this standard is to help LCD manufacturers and panel consumers to better control panel supply and demand cycles, as panels built to these specifications will be able to be used interchangeably without requiring alterations in product tooling or the display module.

### Summary

This standard describes the selected electrical interfaces, mechanical dimensions and data formatting for 10.1-, 11.6-, 13.3-, 13.4-, 14.0-, 15.6-, 17.3-, and 18.4-inch wide format (W) 16:9 panels.

### 2.2.4 LVDS 6-bit I/F Signal Definition (40 pin for LED BL, 2-channel Input with LED Driver in PCB)

The LVDS signal interface cable shall be terminated into an I-PEX 20455-040E-12 or equivalent connector. The interface connector pin assignments are listed in Table 2-4.



~596 Mbps per Differential Lane

### 2.2.4 LVDS 6-bit I/F Signal Definition (40 pin for LED BL, 2-channel Input with LED Driver in PCB)

I-PEX Cabline Connector

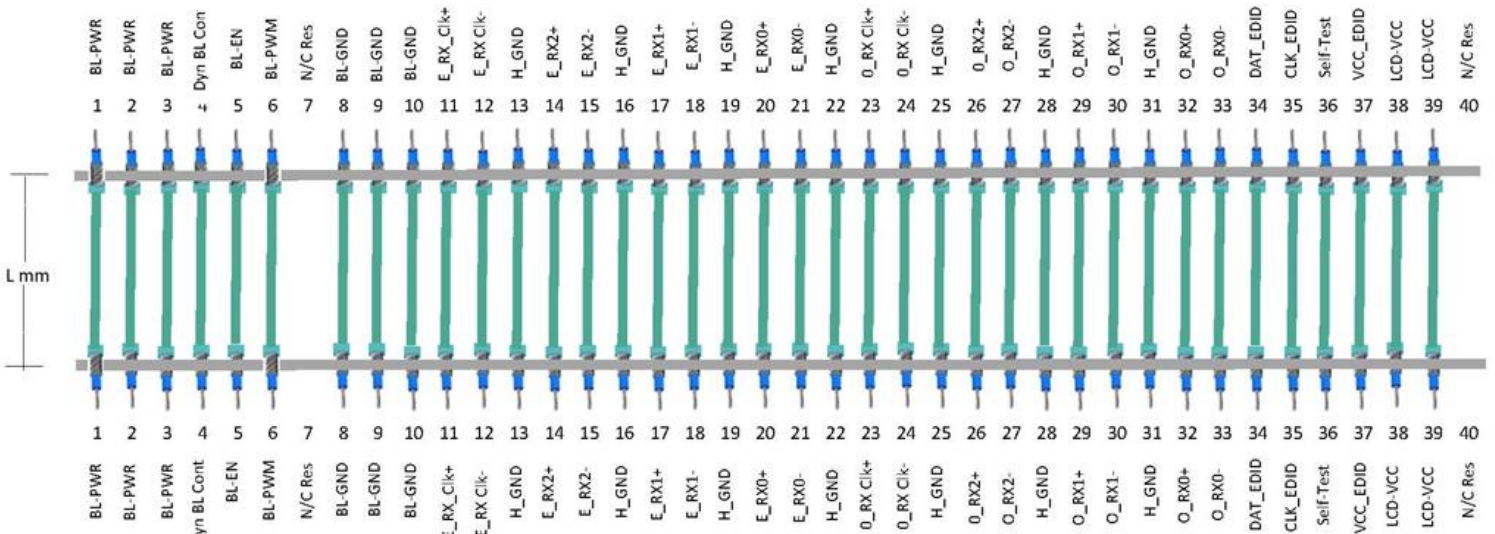
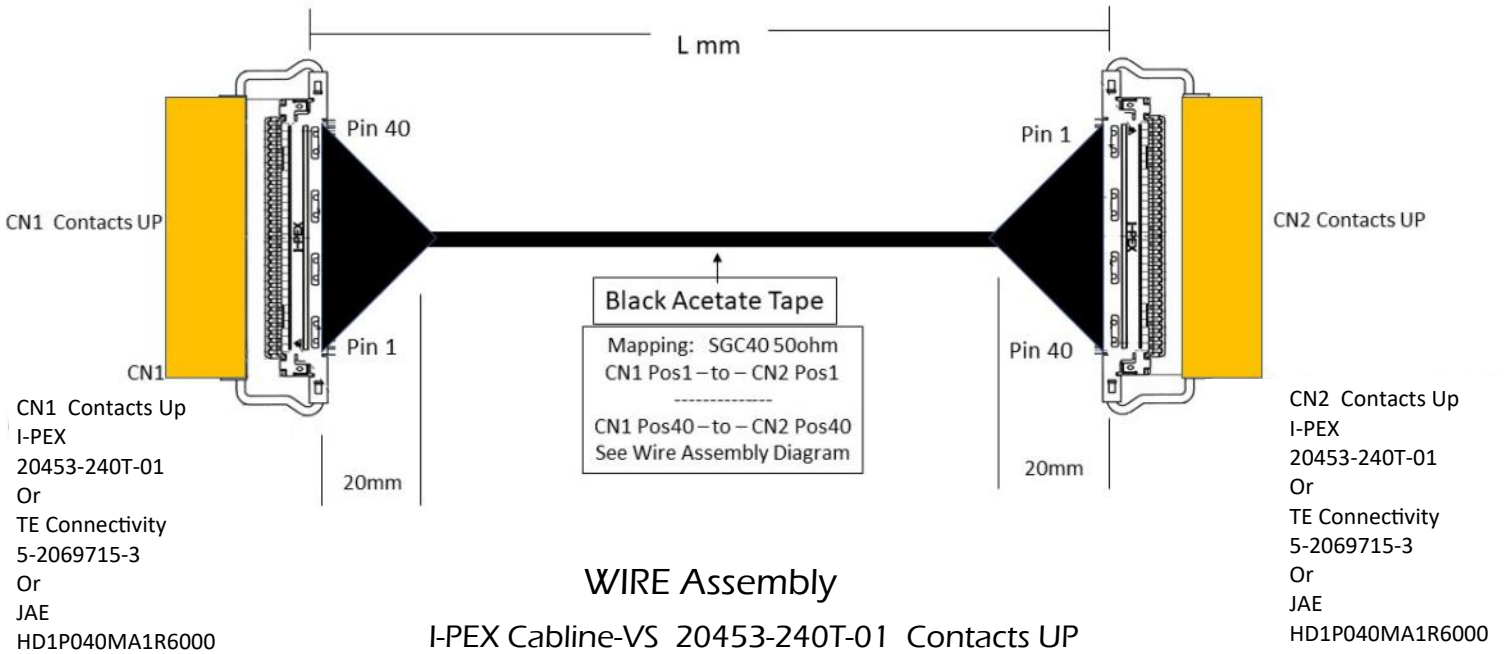
The LVDS signal interface cable shall be terminated into an I-PEX 20455-040E-12 or equivalent connector. The interface connector pin assignments are listed in Table 2-4.

Connector Pin	Pin No.	Symbol	Function
	1	NC-Reserved	Reserved for LCD manufacturer's use
40	2	LCD_VCC	LCD logic and driver power (3.3V typical)
39	3	LCD_VCC	LCD logic and driver power (3.3V typical)
38	4	VCC_EDID	DDC power
37	5	LCD_Self_Test or NC	LCD panel self test enable (optional)
36	6	CLK_EDID	DDC clock
35	7	DAT_EDID	DDC data
34	8	ORX0-	Negative LVDS differential data input for odd pixel
33	9	ORX0+	Positive LVDS differential data input for odd pixel
32	10	H_GND	High speed ground
31	11	ORX1-	Negative LVDS differential data input for odd pixel
30	12	ORX1+	Positive LVDS differential data input for odd pixel
29	13	H_GND	High speed ground
28	14	ORX2-	Negative LVDS differential data input for odd pixel
27	15	ORX2+	Positive LVDS differential data input for odd pixel
26	16	H_GND	High speed ground
25	17	ORXC-	Negative LVDS differential clock input for odd pixel
24	18	ORXC+	Positive LVDS differential clock input for odd pixel
23	19	H_GND or CEE	High speed ground (Color engine enable optional)
22	20	ERX0-	Negative LVDS differential data input for even pixel
21	21	ERX0+	Positive LVDS differential data input for even pixel
20	22	H_GND	High speed ground
19	23	ERX1-	Negative LVDS differential data input for even pixel
18	24	ERX1+	Positive LVDS differential data input for even pixel
17	25	H_GND	High speed ground
16	26	ERX2-	Negative LVDS differential data input for even pixel
15	27	ERX2+	Positive LVDS differential data input for even pixel
14	28	H_GND	High speed ground
13	29	ERXC-	Negative LVDS differential clock input for even pixel
12	30	ERXC+	Positive LVDS differential clock input for even pixel
11	31	BL_GND	Backlight ground
10	32	BL_GND	Backlight ground
09	33	BL_GND	Backlight ground
08	34	NC-Reserved	Reserved for LCD manufacturer's use
07	35	BL_PWM_DIM	System PWM signal input for dimming
06	36	BL_ENABLE	Backlight on/off
05	37	DBC	Dynamic backlight control
04	38	BL_PWR	Backlight power
03	39	BL_PWR	Backlight power
02	40	BL_PWR	Backlight power
01			



~596 Mbps per Differential Lane

M200915B\_C40LVDS\_VS40x2\_1-1\_xxx



Small Gauge Coax SGC40\_50ohm  
Controlled Impedance  
Center Conductor Resistance = 5 Ω/m

Bundle Formula

$$(D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i})$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

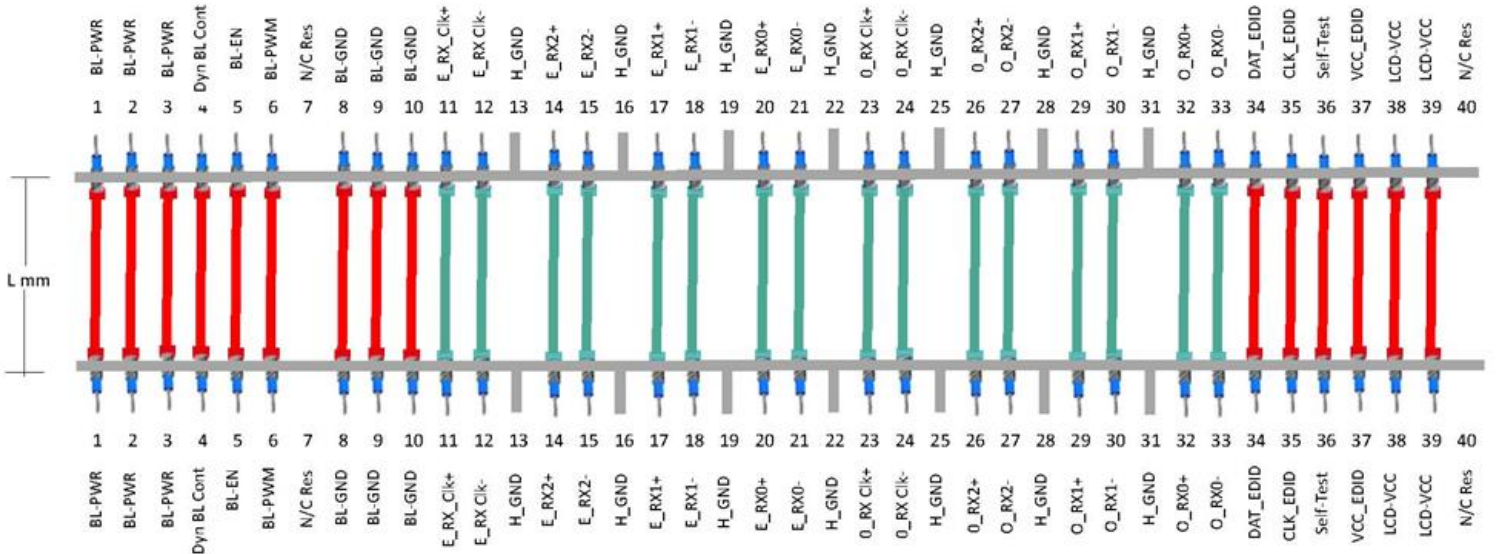
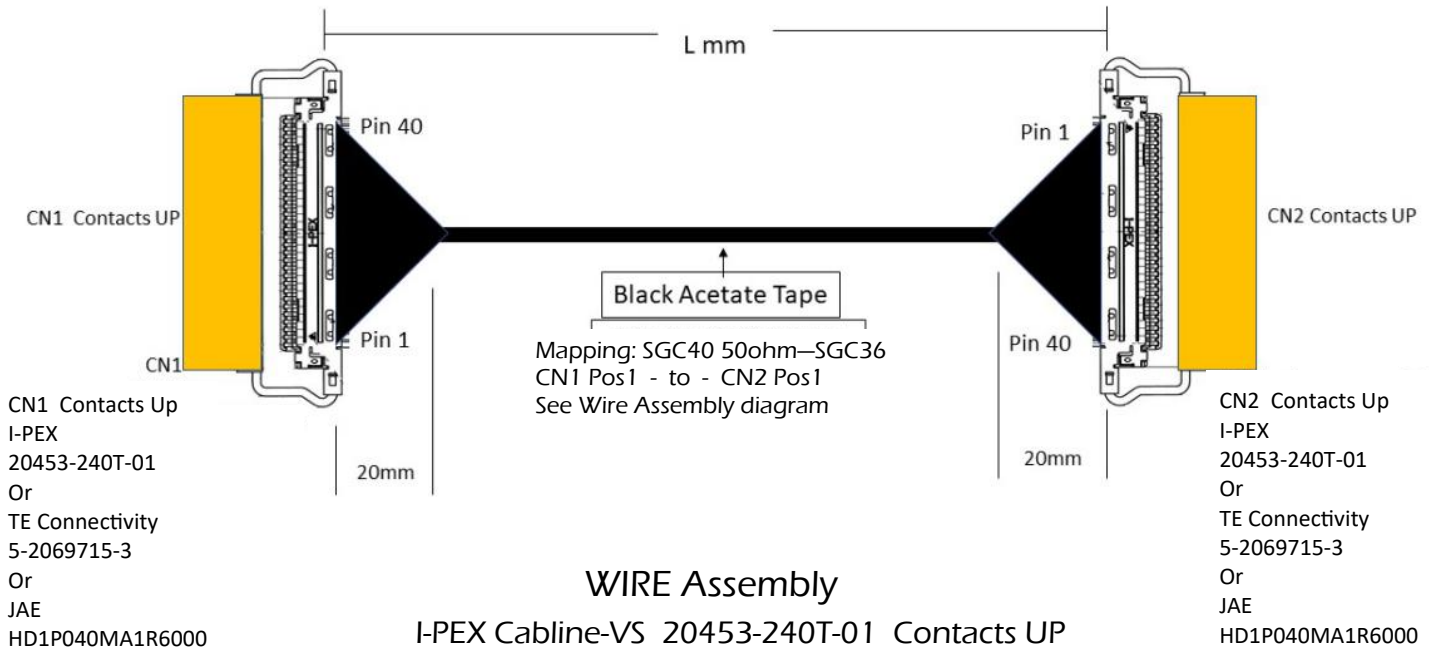
SGC40 50ohm =  $\varnothing 0.36 \pm 0.02$ mm  
Center Conductor Resistance = 5 Ω/m

D =  $\varnothing 2.81$  mm

Est. 180deg. Bending Radius = ~14.1 mm

~596 Mbps per Differential Lane

M20915B\_C40-36LV\_VS40x2\_1-1\_xxx



Small Gauge Coax SGC36  
Non-Controlled Impedance Signals  
Center Conductor Resistance = 1.5 Ω/m

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance Signals

SGC40 50ohm =  $\varnothing 0.36 \pm 0.02\text{mm}$

Bundle Formula

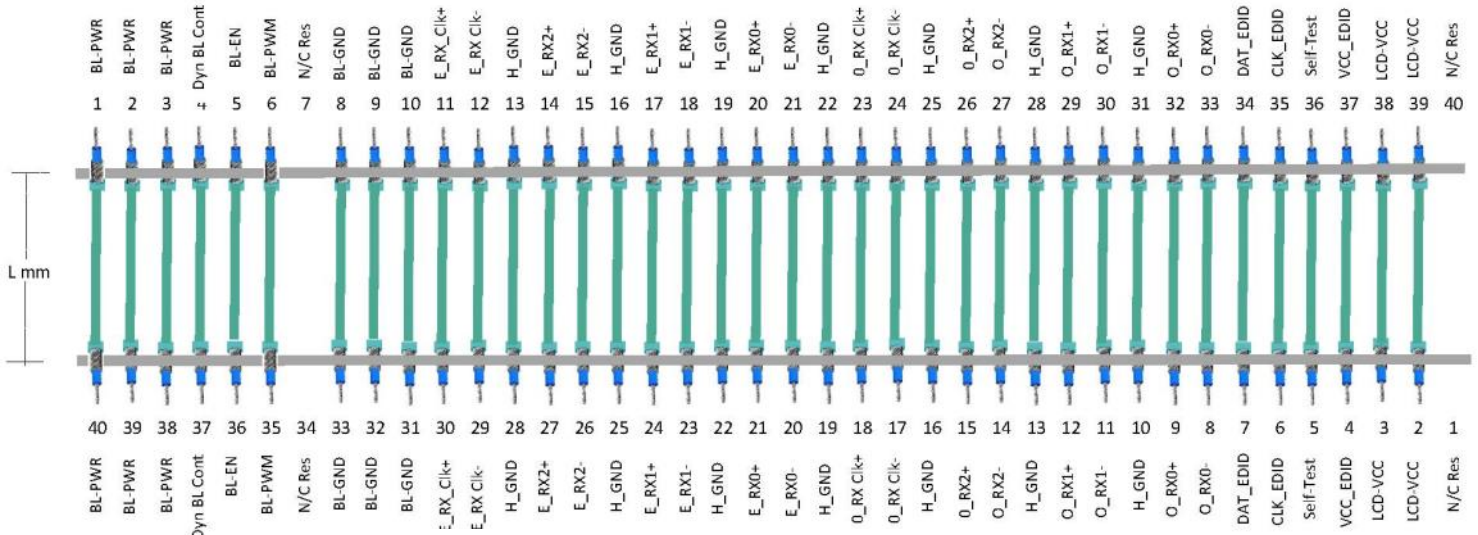
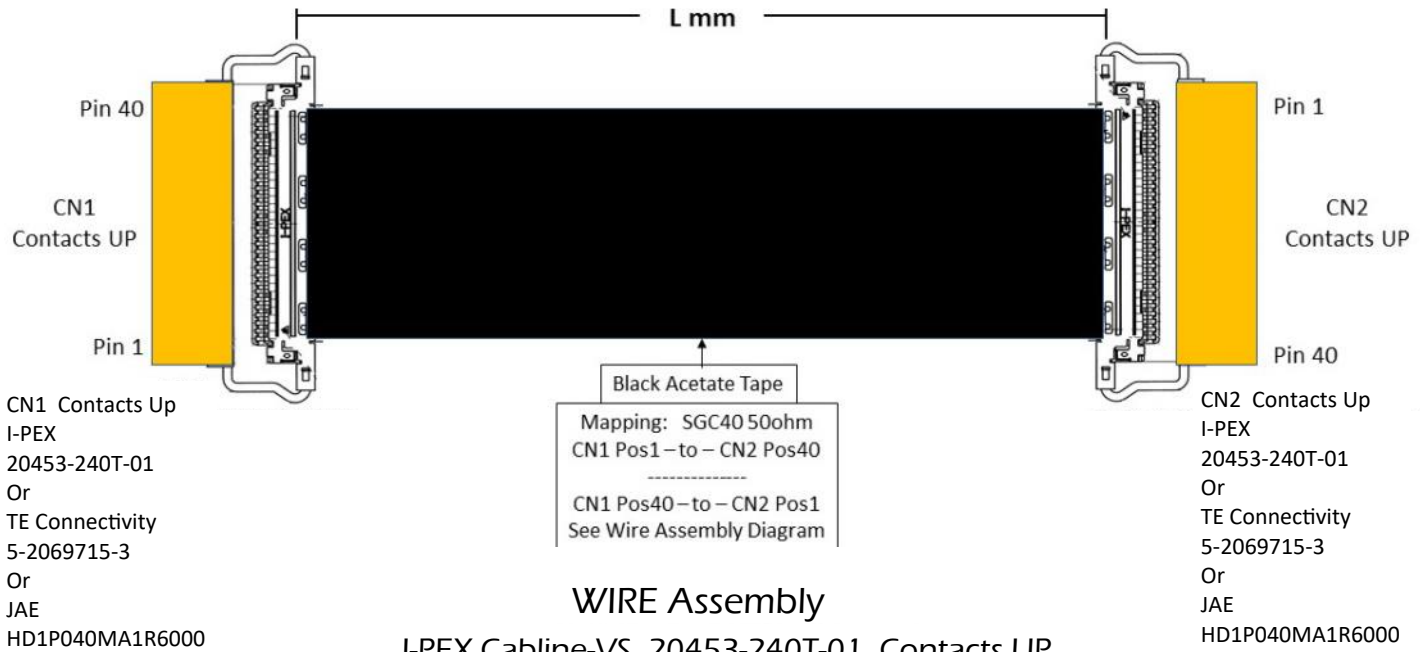
$$(D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i})$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

SGC36 Non-Imp =  $0.365 \pm 0.02$   
Center Conductor Resistance = 1.5 Ω/m  
 $D = \varnothing 2.55 \text{ mm}$   
Est. 180deg. Bending Radius = ~12.8 mm

~596 Mbps per Differential Lane

M200915F\_C40LV\_VS40x2\_1-40\_XXX



I-PEX Cabline-VS 20453-240T-01 Contacts UP

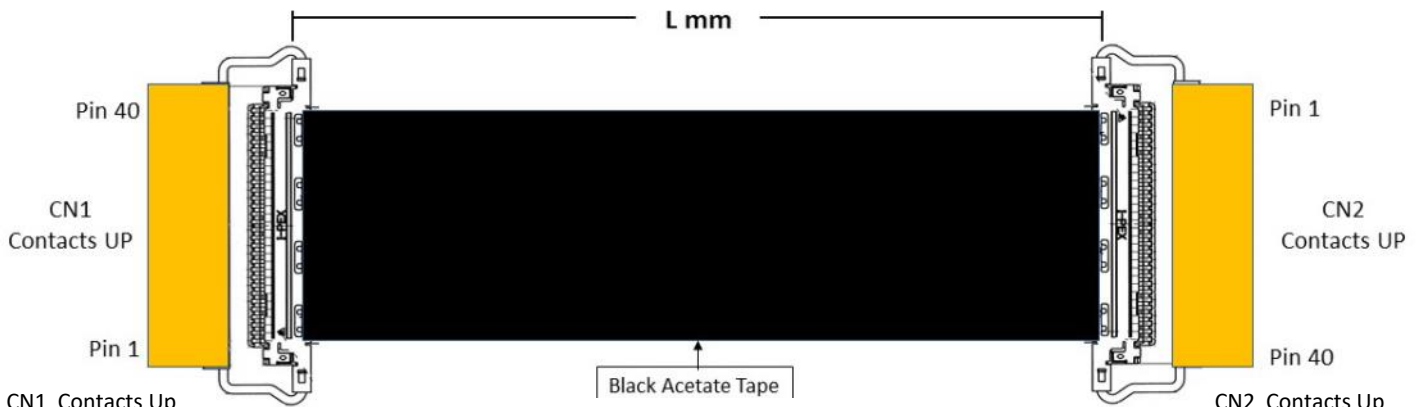
Small Gauge Coax SGC40\_50ohm  
Controlled Impedance  
Center Conductor Resistance = 5 Ω/m

For Power signals: SGC40 Center Conductor Resistance = 5 Ω/m  
180 deg. Bending Radius = ~ 2.5mm



~596 Mbps per Differential Lane

M20915F\_C40-36LV\_VS40x2\_1-40\_xxx



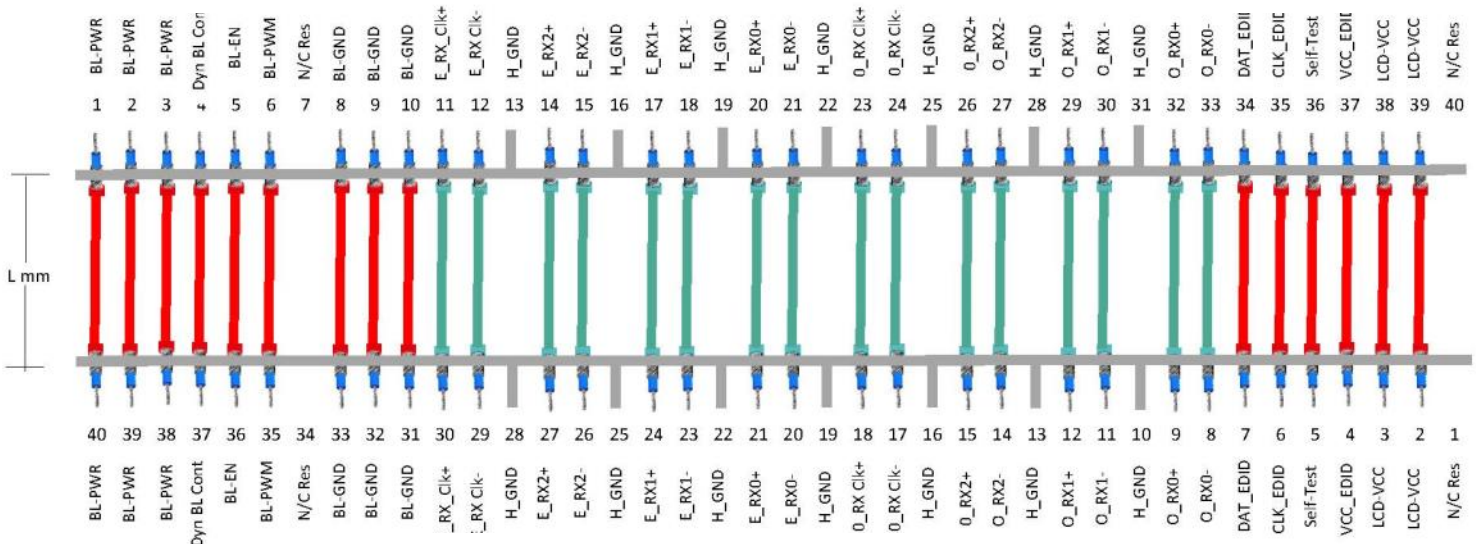
CN1 Contacts Up  
I-PEX  
20453-240T-01  
Or  
TE Connectivity  
5-2069715-3  
Or  
JAE  
HD1P040MA1R6000

Mapping : SGC40-SGC36  
CN1 Pos1 -to- CN2 Pos. 40  
See wire Assembly

CN2 Contacts Up  
I-PEX  
20453-240T-01  
Or  
TE Connectivity  
5-2069715-3  
Or  
JAE  
HD1P040MA1R6000

WIRE Assembly

I-PEX Cabline-VS 20453-240T-01 Contacts UP



I-PEX Cabline-VS 20453-240T-01 Contacts UP

Small Gauge Coax SGC36  
Non-Controlled Impedance Signals  
Center Conductor Resistance = 1.5 Ω/m

Small Gauge Coax SGC40\_50ohm  
Controlled Impedance Signals

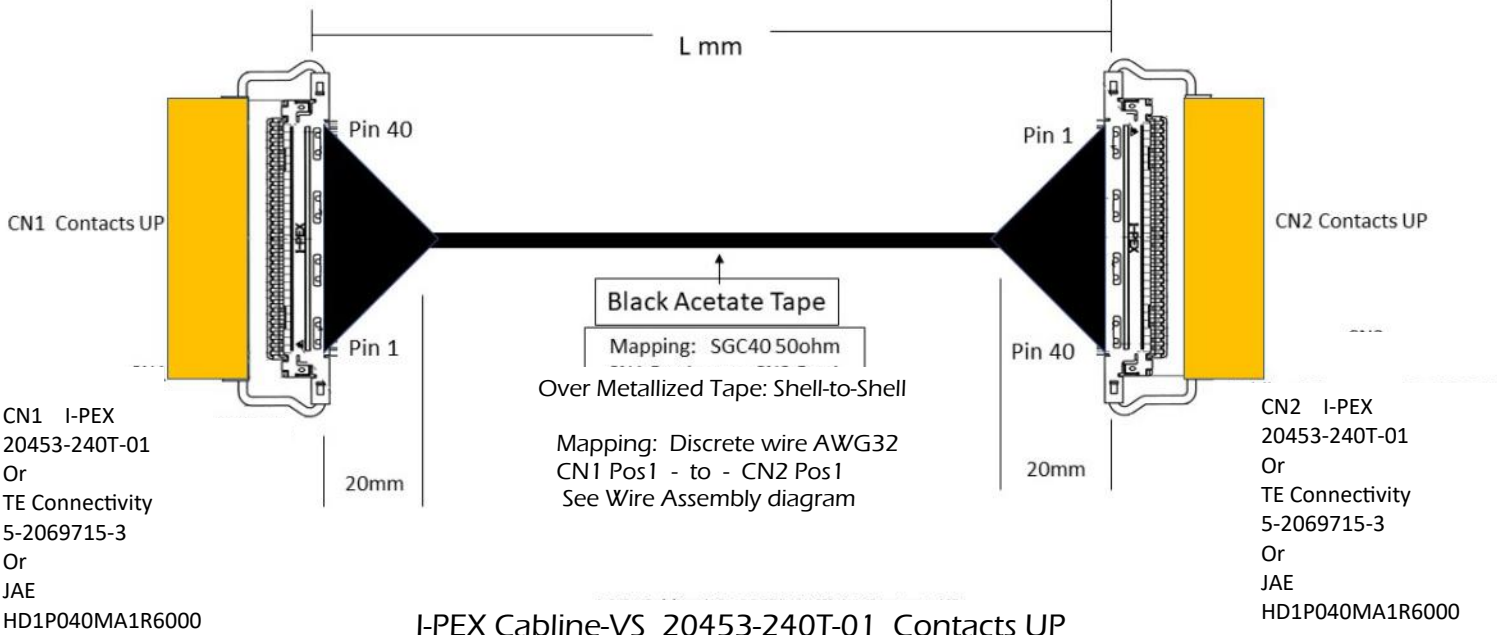
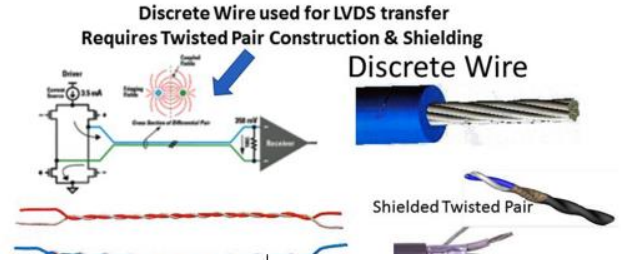
For Power signals: SGC36 (Non-Imp) Center Conductor Resistance = 1.5 Ω/m  
180 deg. Bending Radius = ~ 2.53 mm

# LVDS Technology

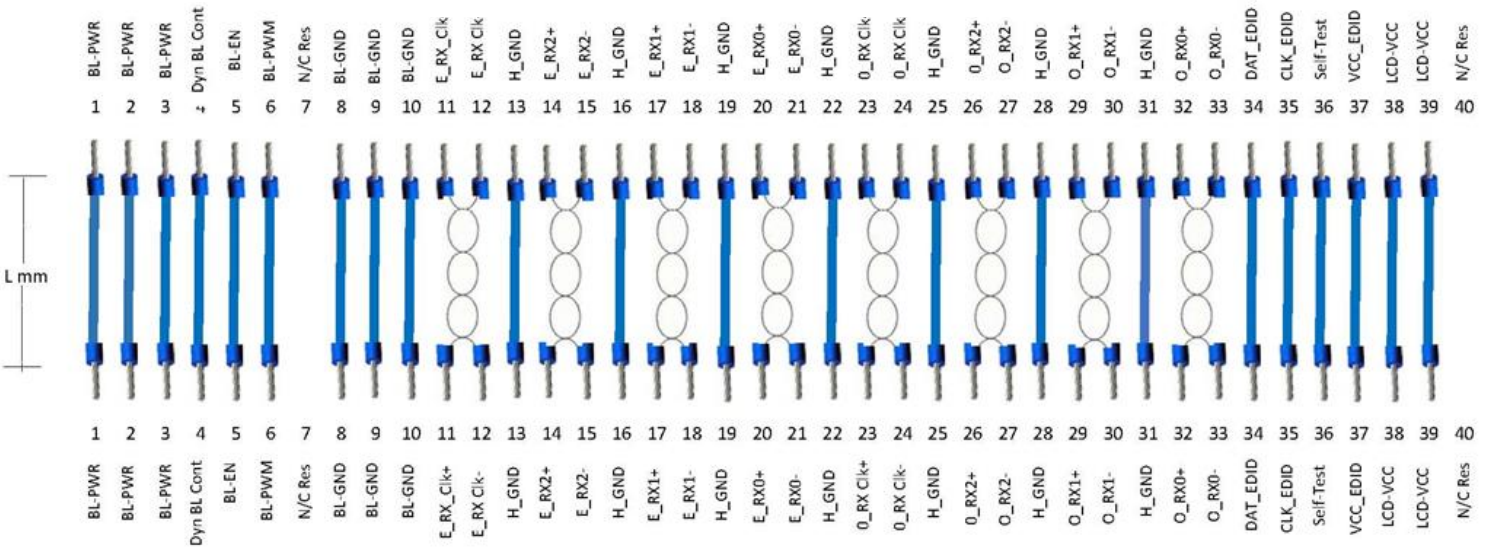
~596 Mbps per Differential Lane

M200915B\_D32LVDS\_VS40x2\_1-1\_XXX

# Discrete Wire—Twisted Pair



I-PEX Cabline-VS 20453-240T-01 Contacts UP



I-PEX Cabline-VS 20453-240T-01 Contacts DOWN

Discrete Wire AWG32  
UL16004  
Center Conductor Resistance : 0.6 Ω/m

Twisted-Pair used for  
Differential Pair Lanes

Bundle Formula

$$(D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i})$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$

Discrete UL10064 AWG32 =  $\varnothing 0.38 \pm 0.03$ mm

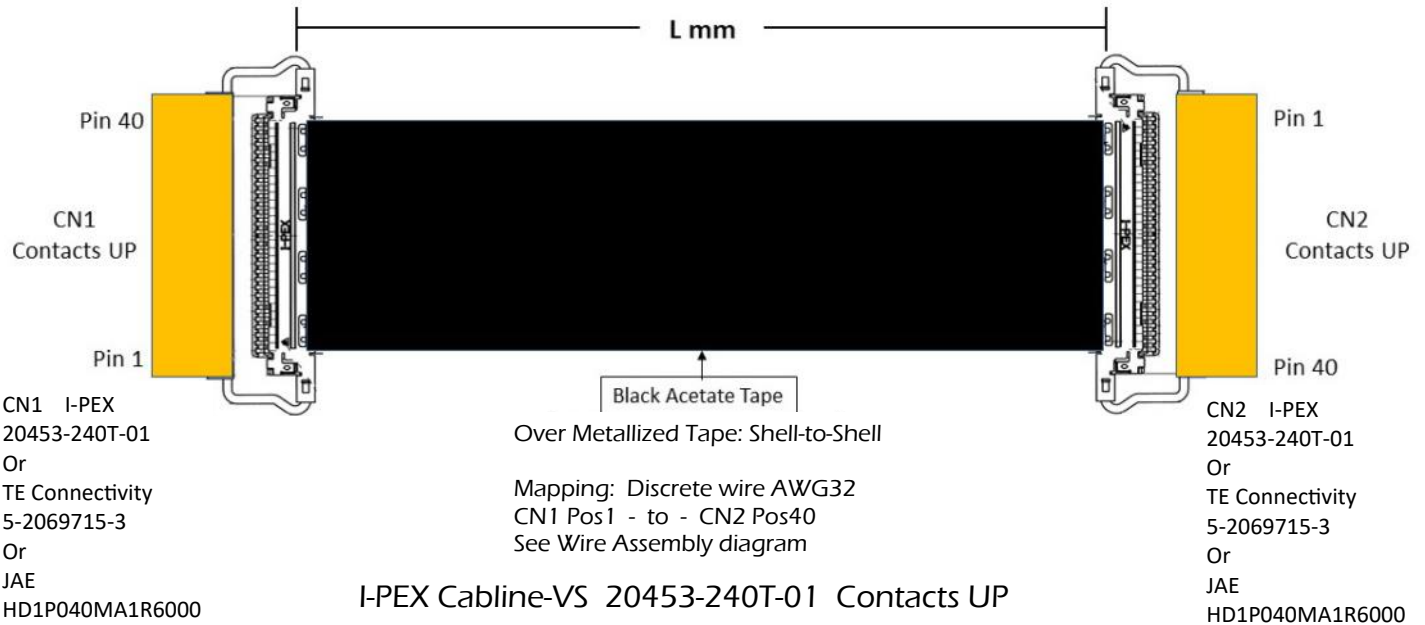
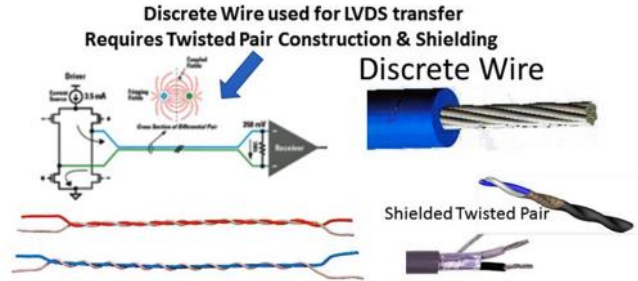
Center Conductor Resistance = 0.6 Ω/m

D =  $\varnothing 3.03$  mm (no tape included)

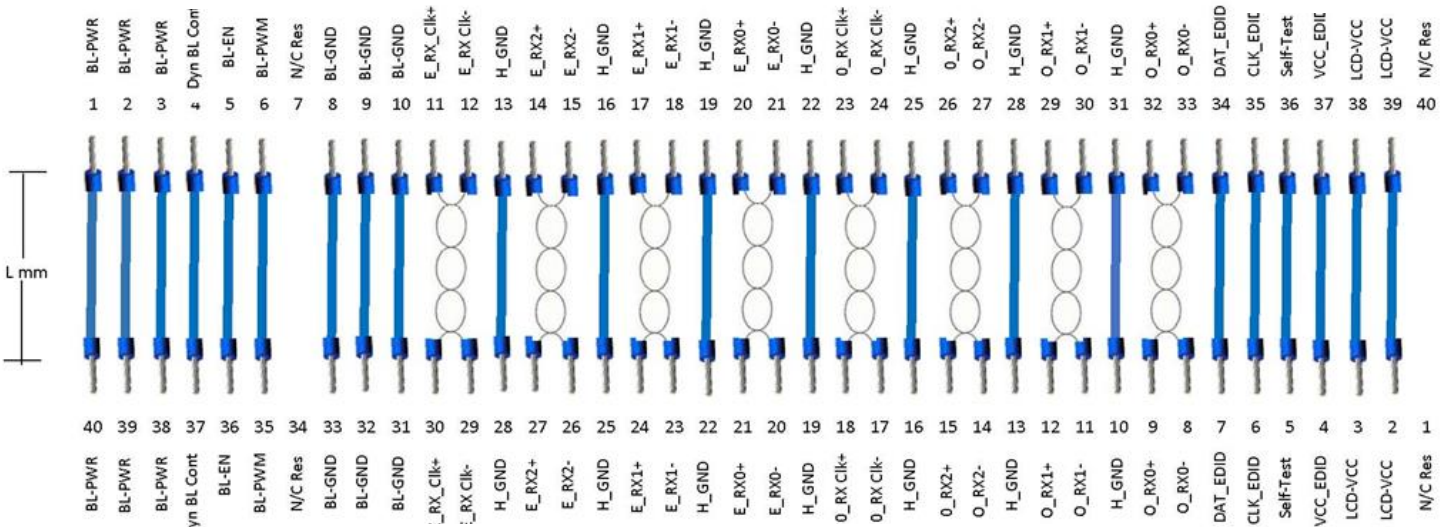
Est. 180deg. Bending Radius = ~15.2 mm

~596 Mbps per Differential Lane

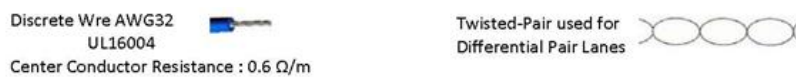
M200915F\_D32LV\_VS40x2\_1-40\_xxx



I-PEX Cabline-VS 20453-240T-01 Contacts UP



I-PEX Cabline-VS 20453-240T-01 Contacts UP



For Power signals: UL10064 AWG32 Center Conductor Resistance = 0.6 Ω/m

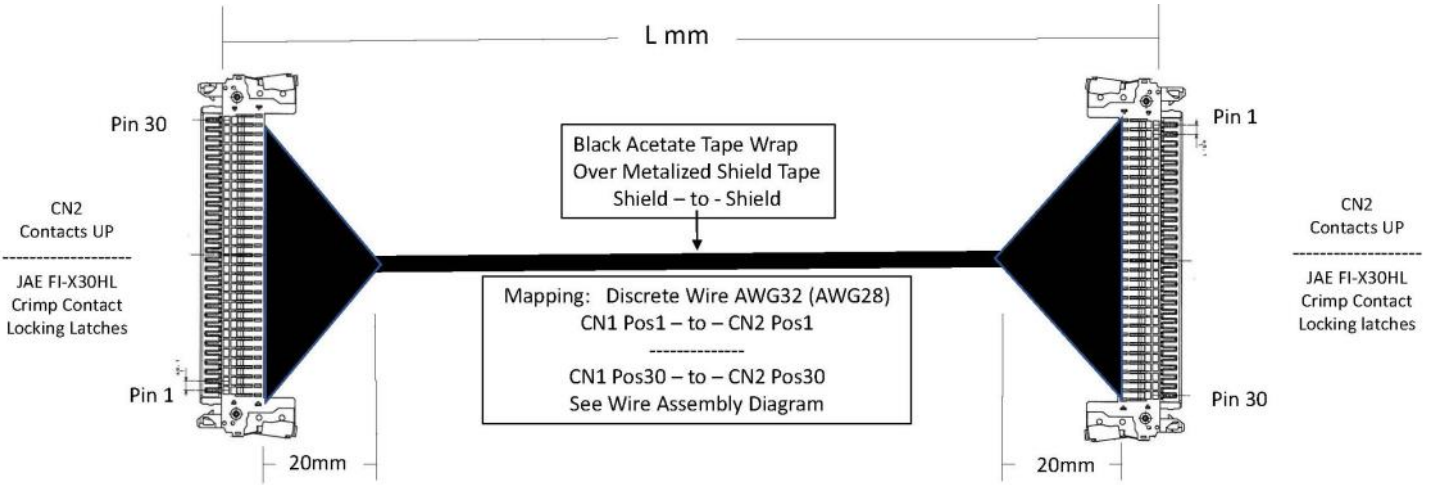


# LVDS Technology 1-1 Bundled Cable Assembly

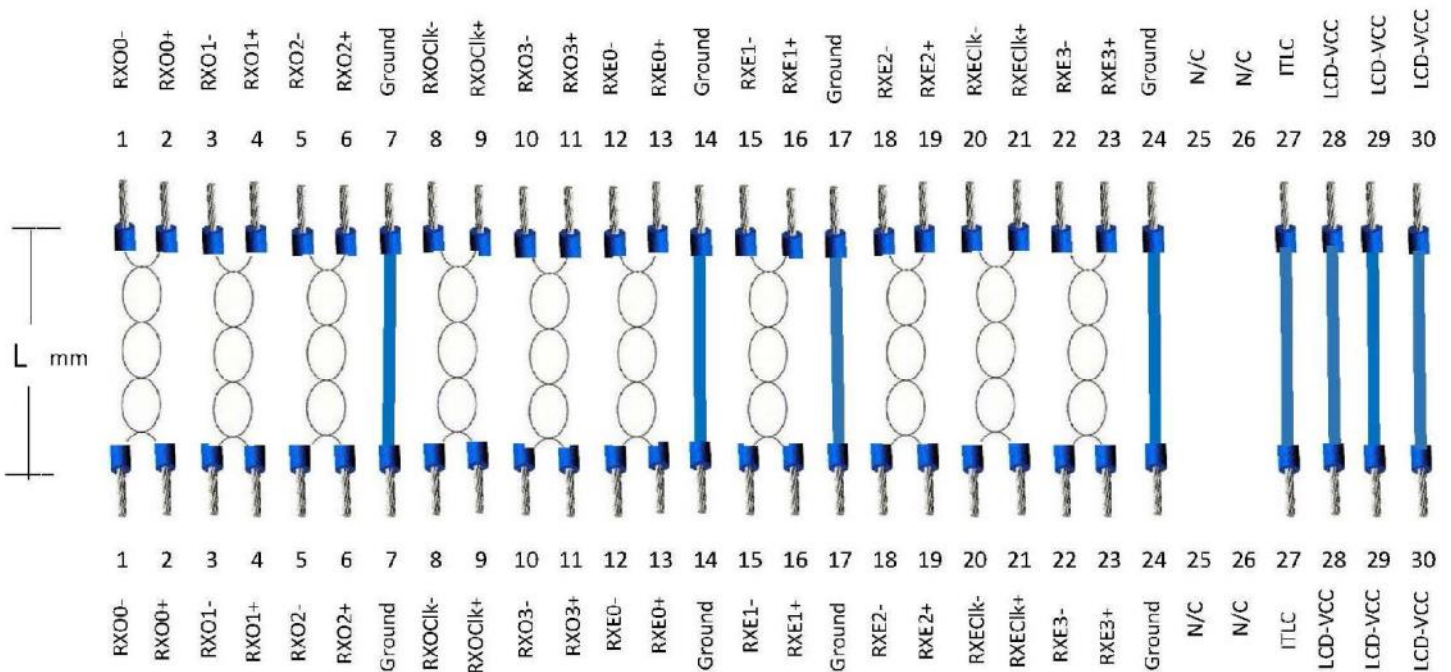
Discrete Wire—  
Twisted Pair  
Locking

~596 Mbps per Differential Lane

M200915B\_D28\_FIX30HLx2\_1-1\_XXX



CN1 JAE FI-X30HL x2 crimp Contacts UP



Note: Discrete Wire AWG28 is commonly used in this application.

CN2 JAE FI-X30HL x2 crimp Contacts DOWN

Twisted-Pair used for Differential Pair Lanes  
100 ohm Controlled



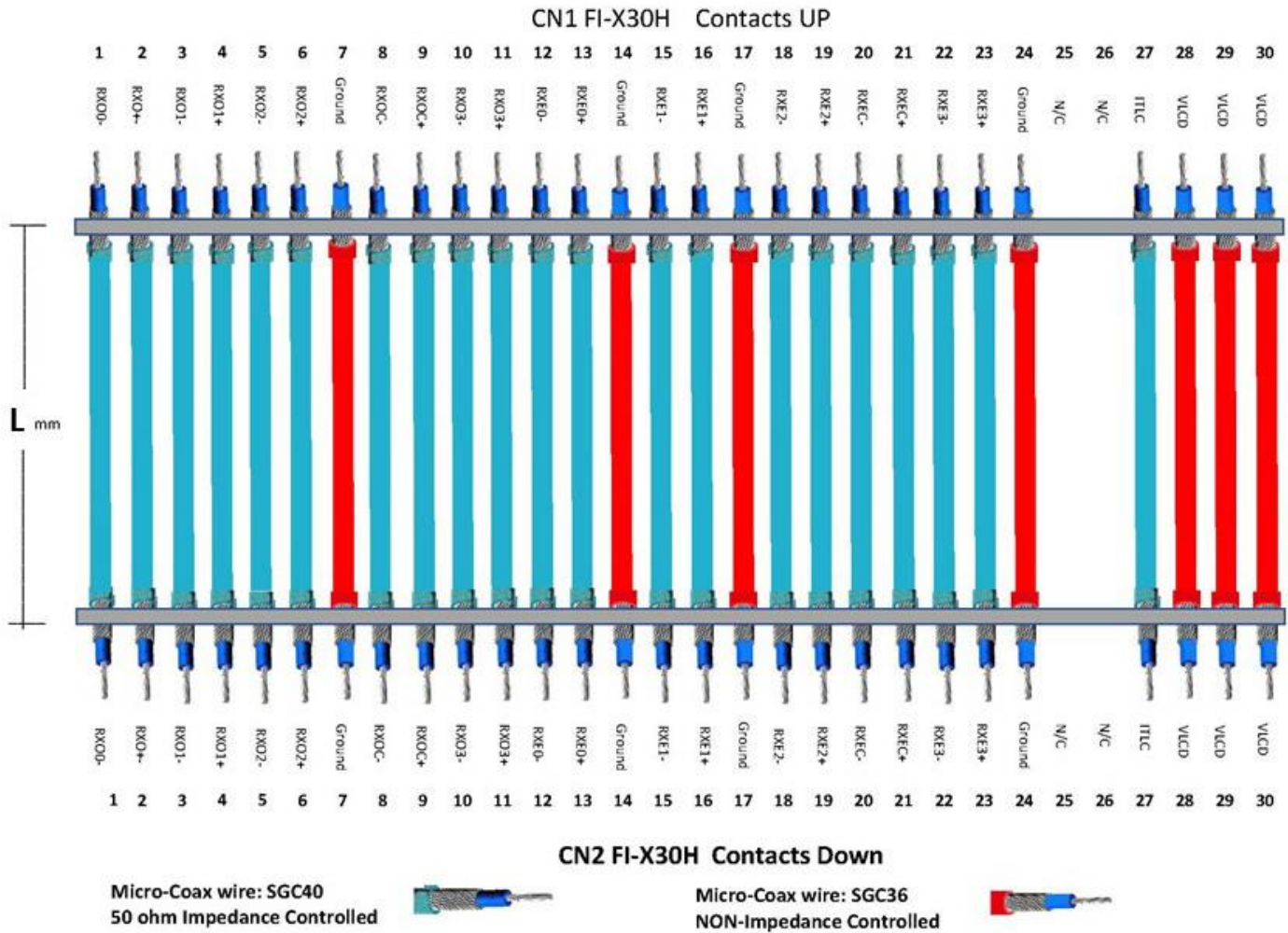
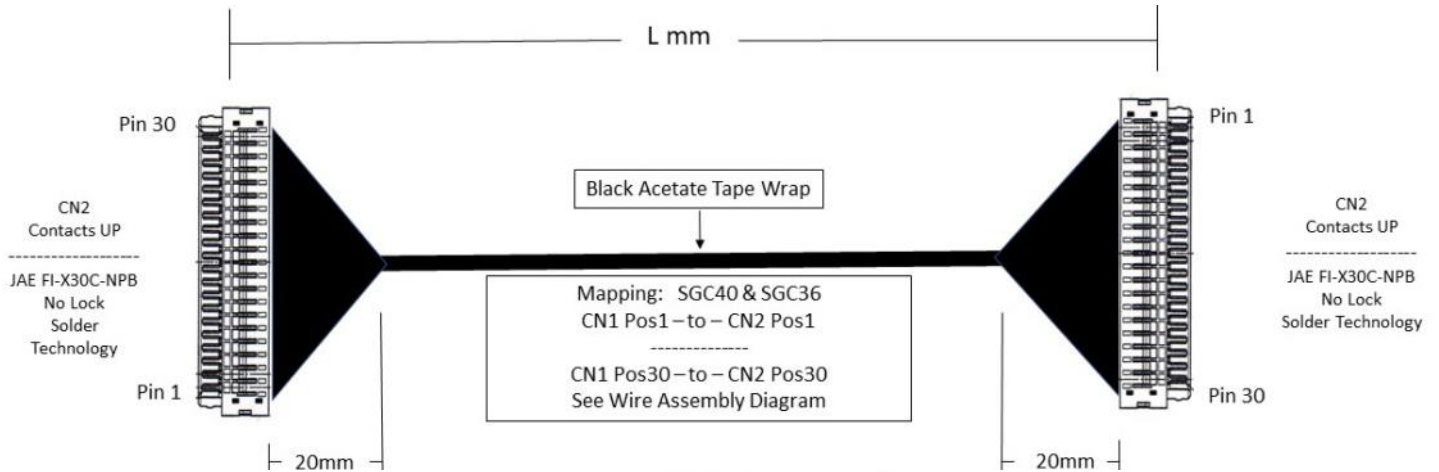
### Bundle Formula

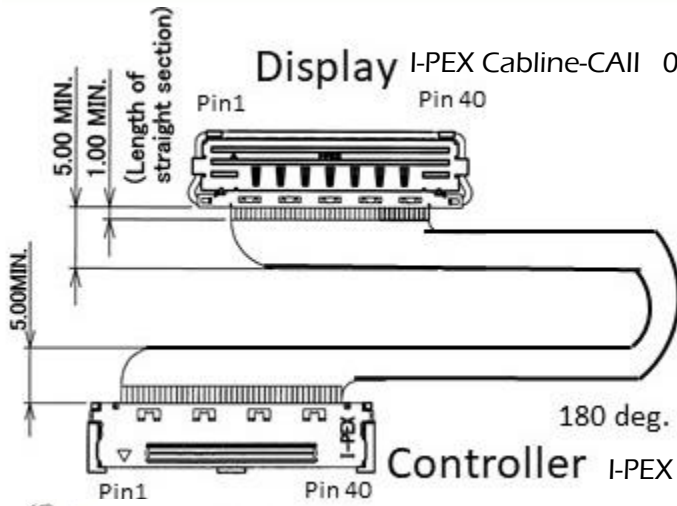
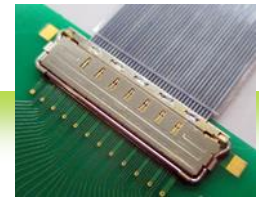
$$D = \sqrt{[(\sum d_i^2)] + \sum \Delta t_i}$$

$$D = 1.2 \sqrt{Q_1 d_1^2 + Q_2 d_2^2 + Q_3 d_3^2 \dots}$$



M20915B\_C40-36\_FIX30Cx2\_1-1\_XXX



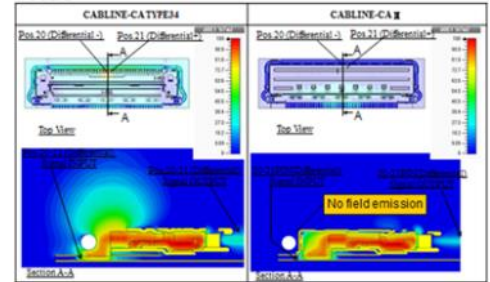


Display I-PEX Cabline-CAII 0.4mm Pitch Full shielded Horizontal Mate Connector

Diameter  $\varnothing = \sim 2.53\text{mm}$

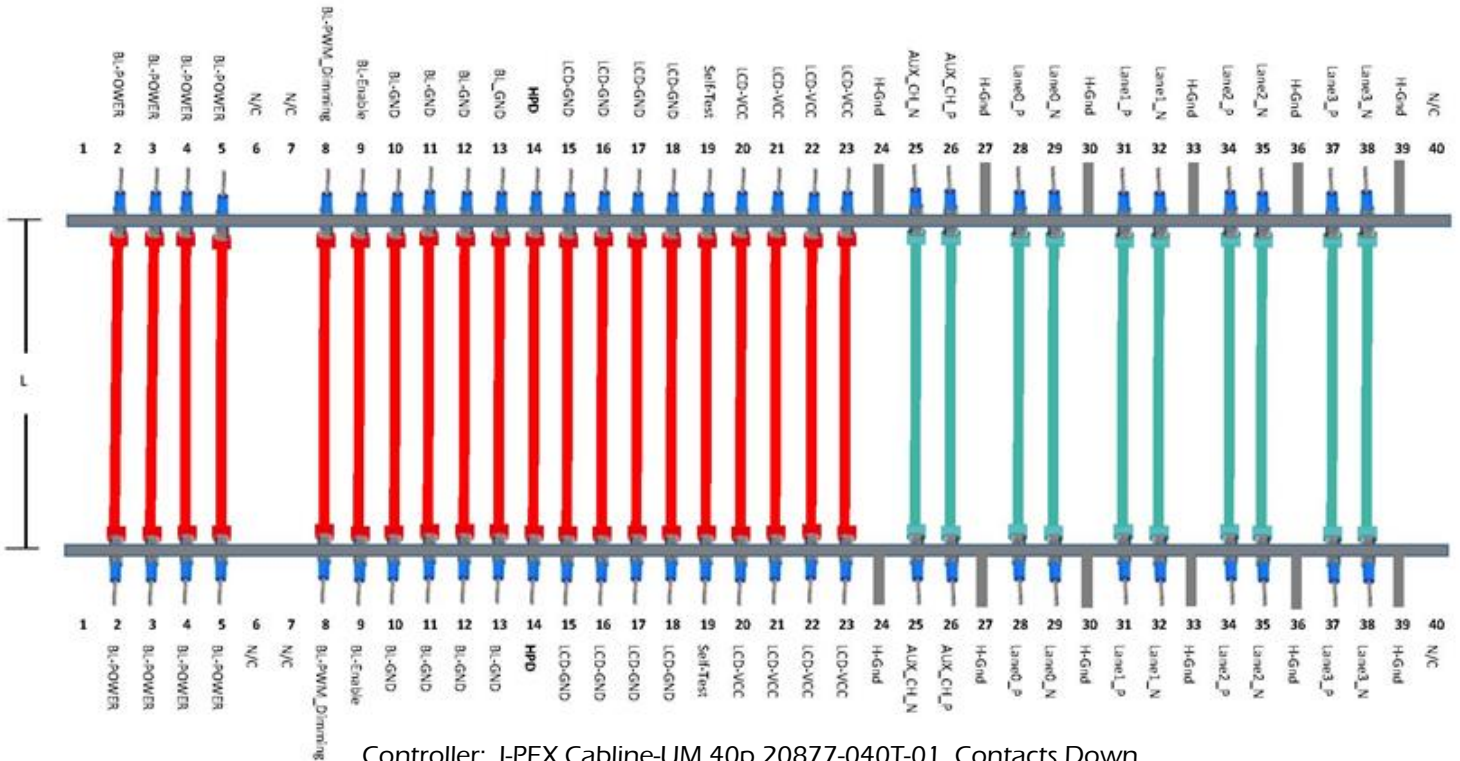
180 deg. Bending radius  $\sim 12.66\text{mm}$

Controller I-PEX Cabline-UM 0.4mm Pitch Full shielded Vertical mate



ABLINI-CAII 40p 20679 Contacts UP

Display : I-PEX Cabline-CAII 40p 20679 Contacts UP



Controller: I-PEX Cabline-UM 40p 20877-040T-01 Contacts Down

Micro-Coaxial wire: SGC36  
For NON Impedance Controlled Signals

Micro-Coaxial wire: SGC40 500  
For Impedance Controlled Signals







North American Engineering and Sales Services for High Speed and General Custom Cables from



**SHAOGUAN Mechanical Reliability & Quality Assurance Equipment**



Constant Temperature & Humidity Chamber



Thermal Shock



Circulation Heating Chamber



Salt Fog Chamber



Bending/twisting Test



Insertion/Extraction Force



Insertion/Extraction "Life" measurements



Temperature Rise Measurements



Mixed flowing GAS



X-Ray Analysis x430 Magnification Shimadzu SMX-130 30W



Spectrophotometer Minolta CM-3700d 360-740nmeter



Fluorescence Line Analysis Oursstex 150RoHS to 8ppm



Digital Microscope Keyence VHX-600 54 milli-pixel 3DCCD

**OPEN SOURCING – Connectors & Wire Suppliers**



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